


# Latitude3000 Schematic

## Haswell-ULT

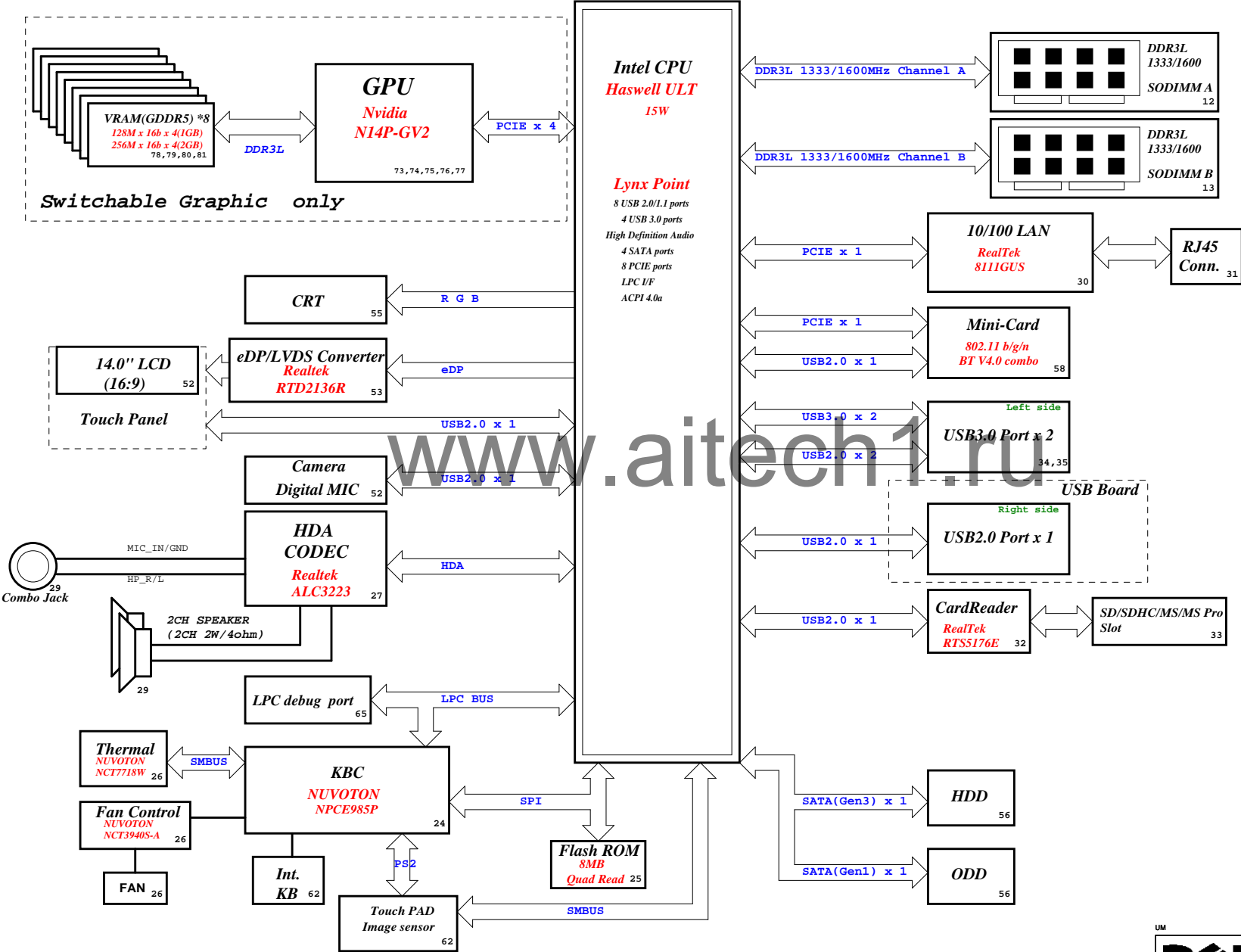
2013-3-15  
REV : X00

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*DY : None Installed*  
*UMA: UMA only installed*  
*OPS: DISCRTE OPTIMUS installed*

|  |  |
|--|--|
| UM   |  |
|                 |  |
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| Title  |  |
| Cover Page   |  |
| Size<br>A3   | Document Number<br>Latitude300 Haswell |
| Date: Friday, March 15, 2013   | Rev<br>X00                             |
| Sheet 1 of 104   |  |

Latitude3000 Block Diagram



| CHARGER   |  |
|---|--|
| BQ24717   | 44   |
| INPUTS  | OUTPUTS  |
| AD+   | DCBATOUT   |
| BT+   |  |
| SYSTEM DC/DC  |  |
| TP851225  | 45   |
| INPUTS  | OUTPUTS  |
| DCBATOUT  | 3D3V_AUX_S5<br>5V_AUX_S5<br>5V_S5<br>3D3V_S5   |
| CPU Core Power                                      |  |
| ISL95813  | 46,47  |
| INPUTS  | OUTPUTS  |
| DCBATOUT  | VCC_CORE   |
| DDR3L SUS   |  |
| TP851216  | 49   |
| INPUTS  | OUTPUTS  |
| DCBATOUT  | 1D35V_S3<br>0D65V_S0   |
| CPU 1.05V   |  |
| RT8237  | 48   |
| INPUTS  | OUTPUTS  |
| DCBATOUT  | 1D05V_S0   |
| CPU 1D5V_S0   |  |
| TLV70215  | 51   |
| INPUTS  | OUTPUTS  |
| 3D3V_S5   | 1D5V_S0  |
| Switches  |  |
| 36  | 83   |
| INPUTS  | OUTPUTS  |
| 1D35V_S3<br>5V_S5<br>3D3V_S5<br>VCCP_CPU<br>3D3V_S0 | 1D35V_S0<br>5V_S0<br>0D675V_S0<br>3D3V_S0<br>1D05V_VGA_S0<br>3D3V_VGA_S0<br>1D35V_VGA_S0 |
| PCB LAYER   |  |
| L1:Top<br>L2:GND<br>L3:Signal<br>L4:Signal          | L5:VCC<br>L6:Signal<br>L7:GND<br>L8:Bottom   |

(Blanking)

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**X00**

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**SSID = CPU**



**Layout Note:**  
Impedance control:50 ohm

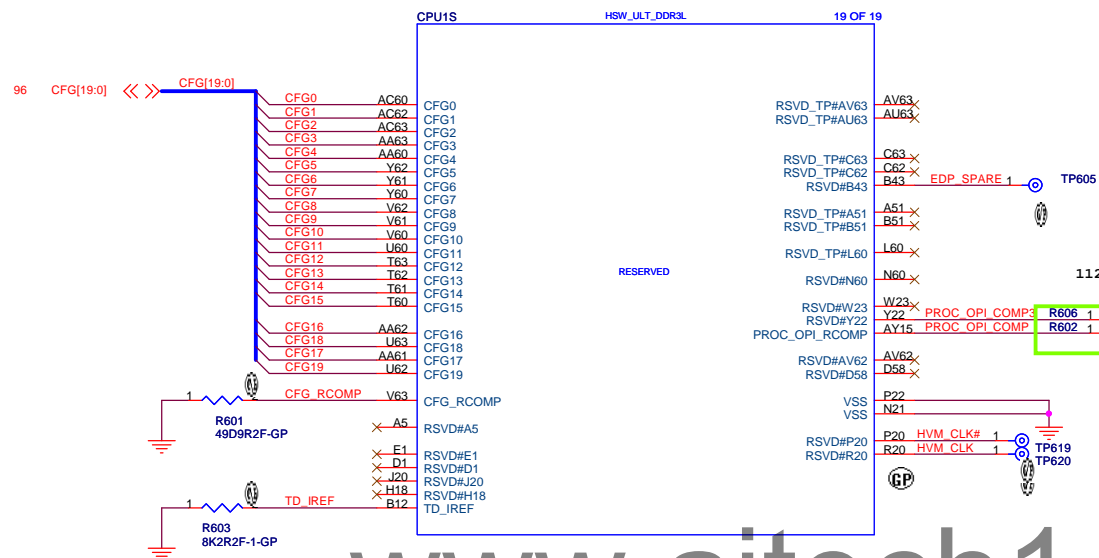


SM\_RCOMP keep routing length less than 500 mils.

— **Layout Note:**  
Place close to DIMM



SSID = CPU

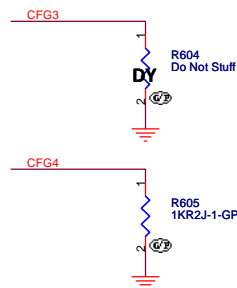


1127 add (follow EA40)

Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

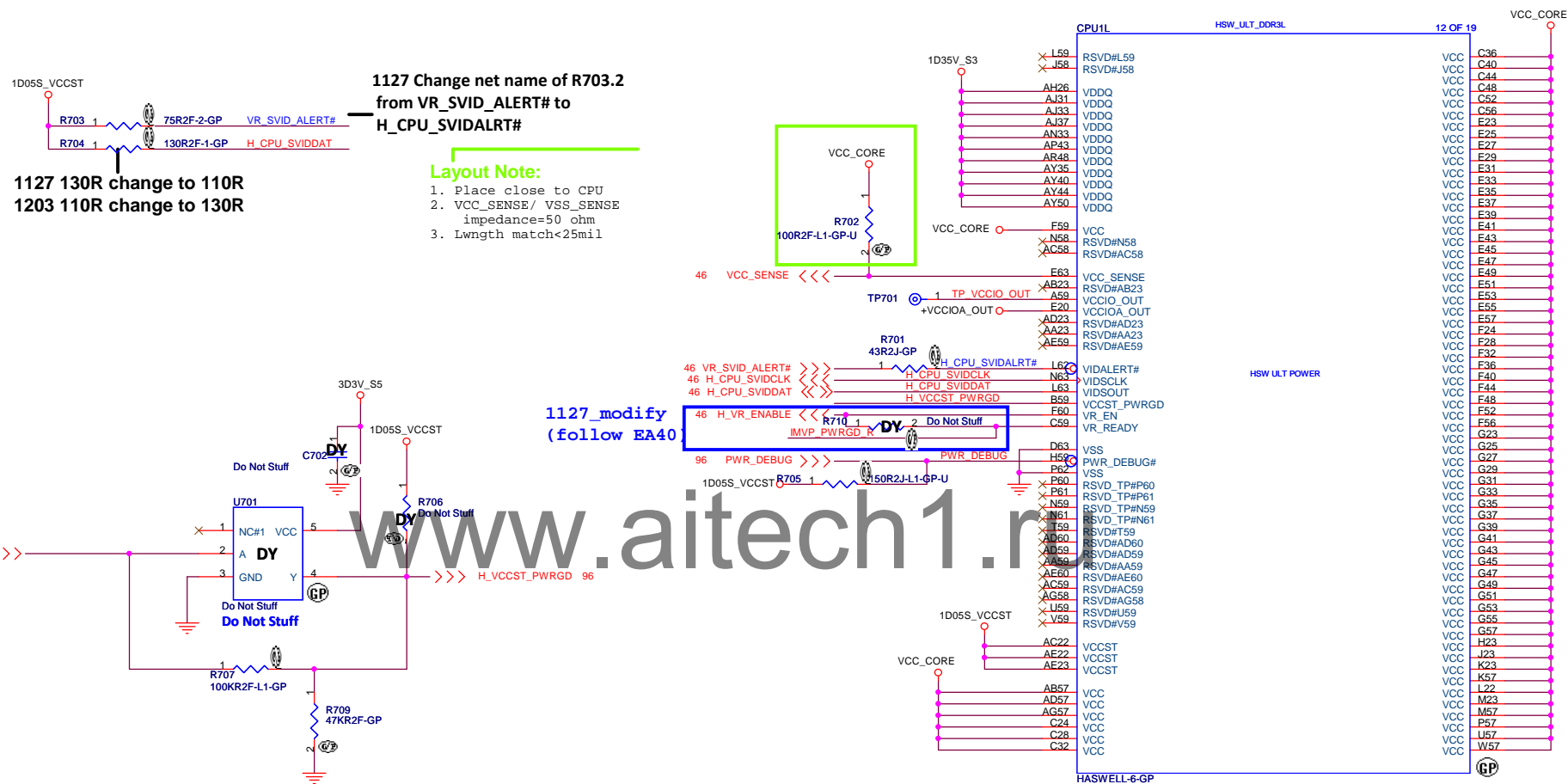
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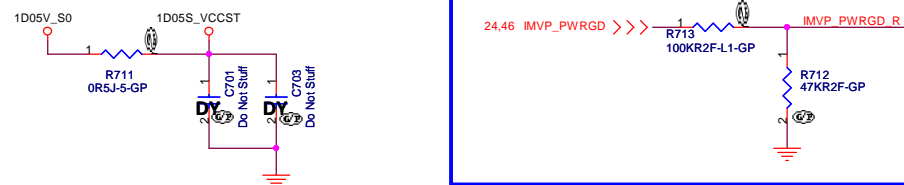
| PHYSICAL_DEBUG_ENABLED (DFX PRIVACY) |   |
|--------------------------------------|---|
| CFG[3]                               | 0 : ENABLED<br>SET DFX ENABLED BIT IN DEBUG INTERFACE MSR<br>1 : DISABLED |

| DISPLAY PORT PRESENCE STRAP |  |
|-----------------------------|--|
| CFG[4]                      | 0 : ENABLED<br>AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT<br>1 : DISABLED<br>NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT |

**SSID = CPU**

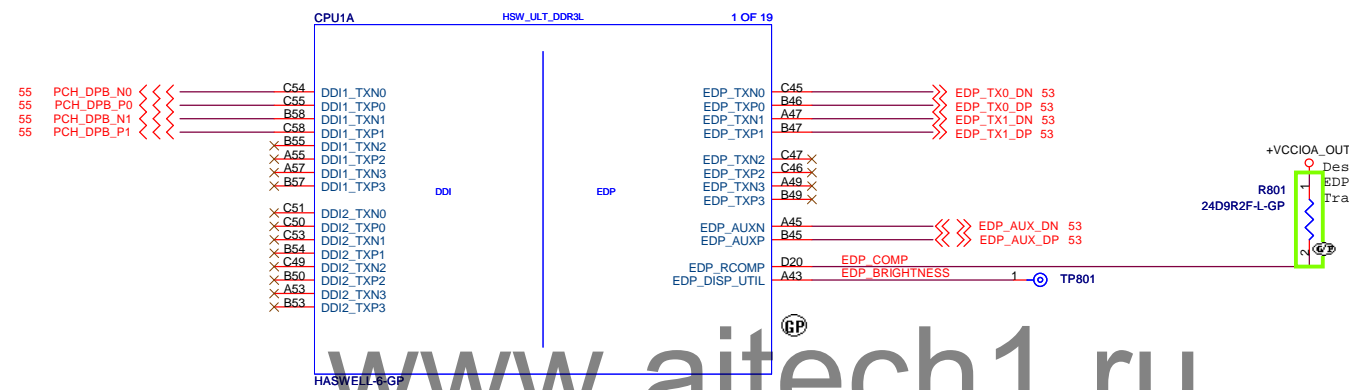


1205 Add



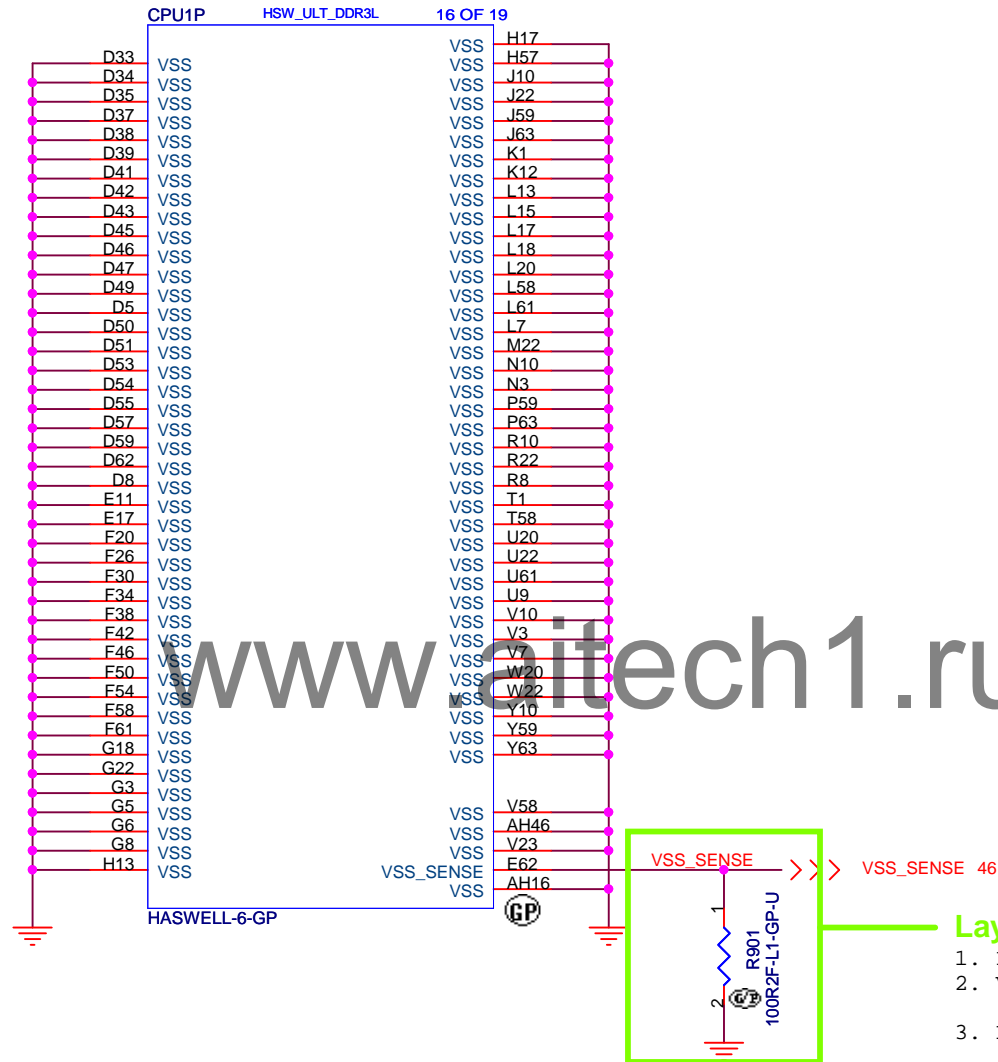
SSID = CPU

CRT



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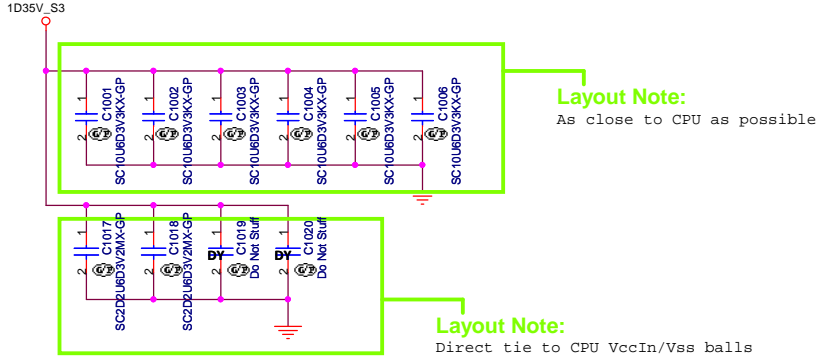
SSID = CPU



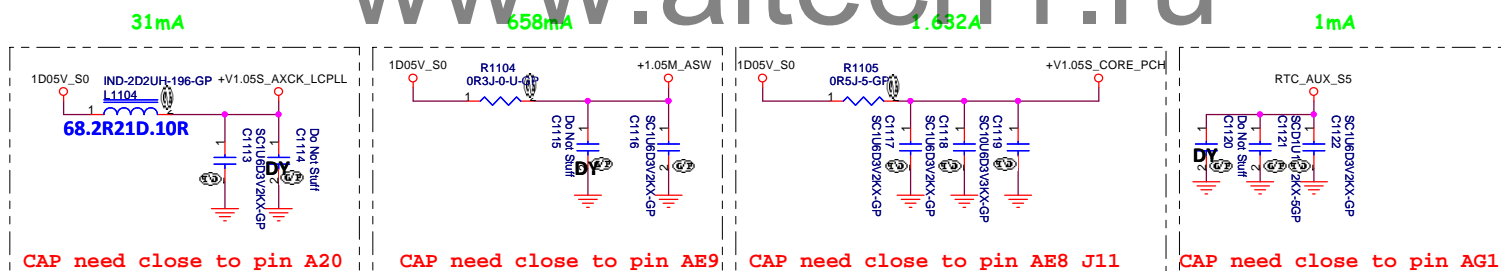
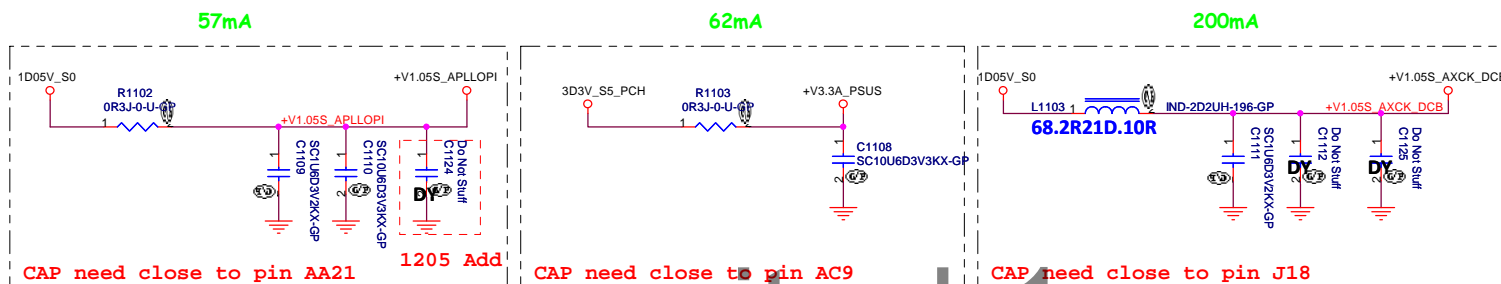
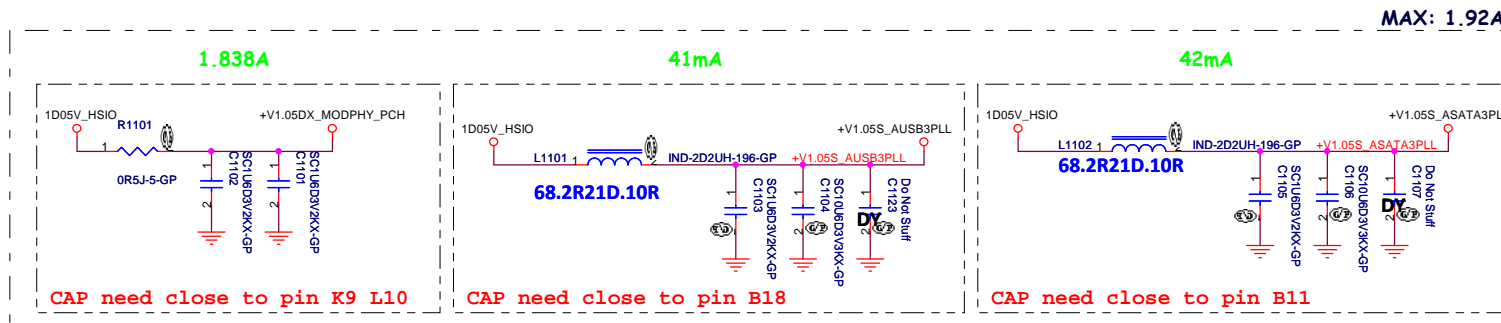
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|                              |                 |   |                   |
|------------------------------|-----------------|---|-------------------|
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| Title                        |                 |   |                   |
| <b>CPU (VSS)</b>             |                 |   |                   |
| Size<br>A4                   | Document Number |   | Rev<br><b>X00</b> |
| <b>Latitude300 Haswell</b>   |                 |   |                   |
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SSID = CPU



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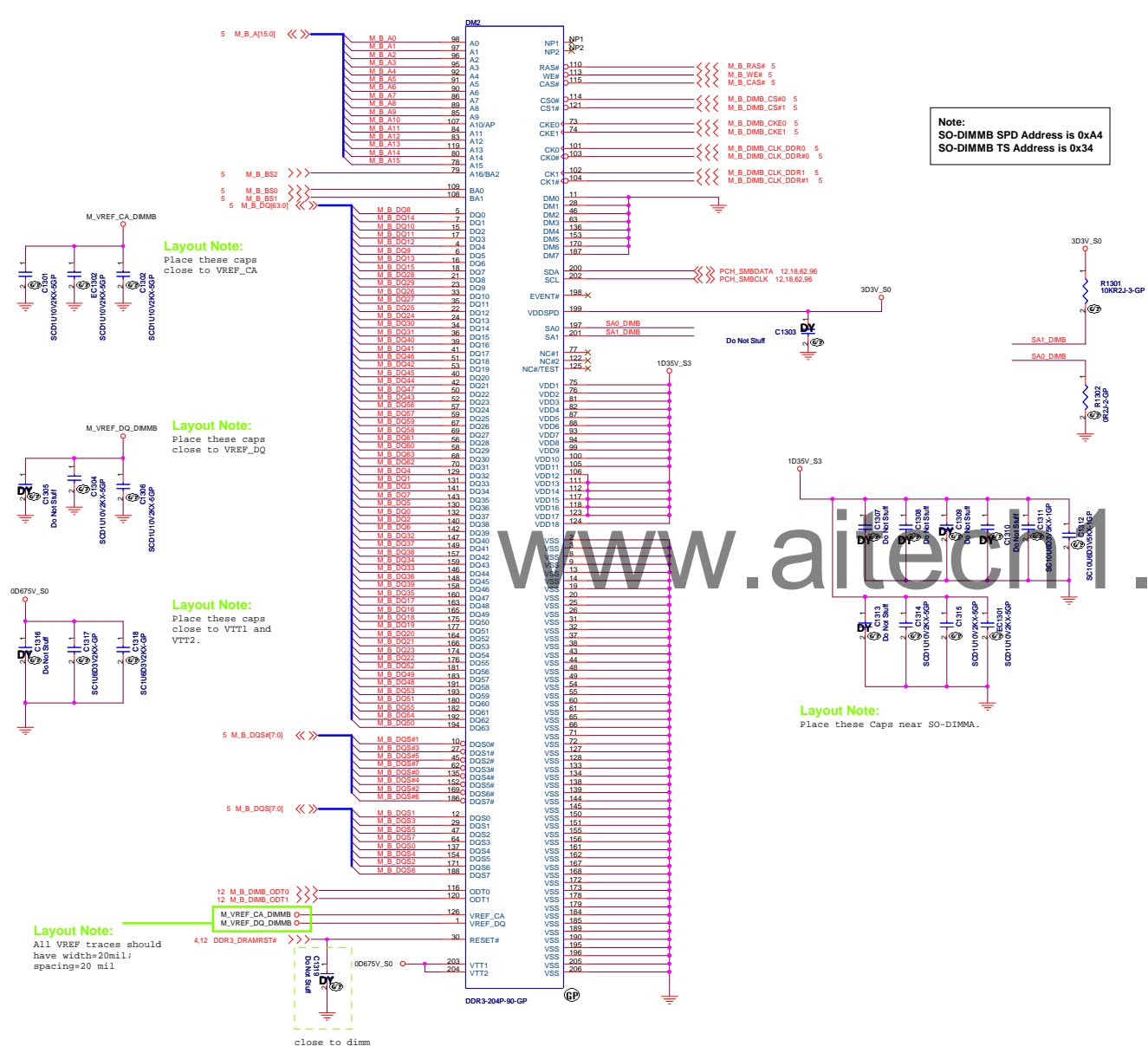


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|       |                        |       |           |
|-------|------------------------|-------|-----------|
| Title |                        |       | Reserved  |
| Size  | Document Number        | Rev   |           |
| A3    | Latitude300 Haswell    | X00   |           |
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Size  
A3

Document Number  
**Latitude300 Haswell**

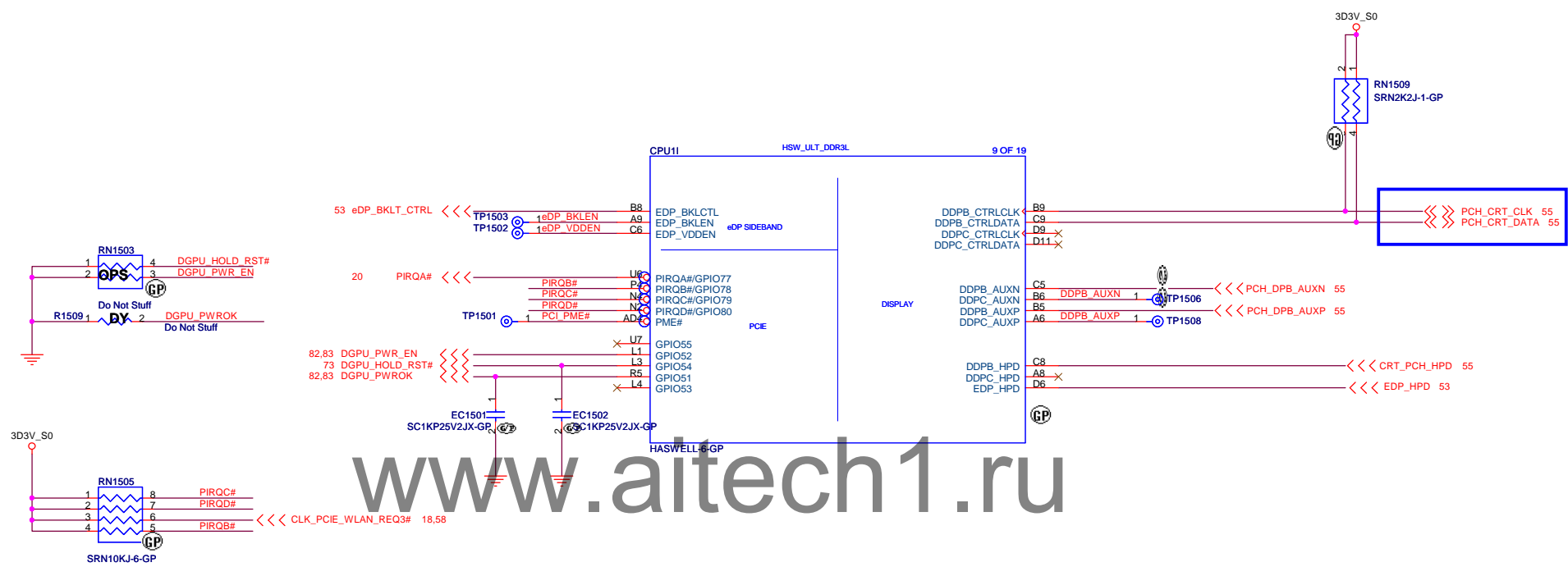
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**M3**

**X00**

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SSID = CPU



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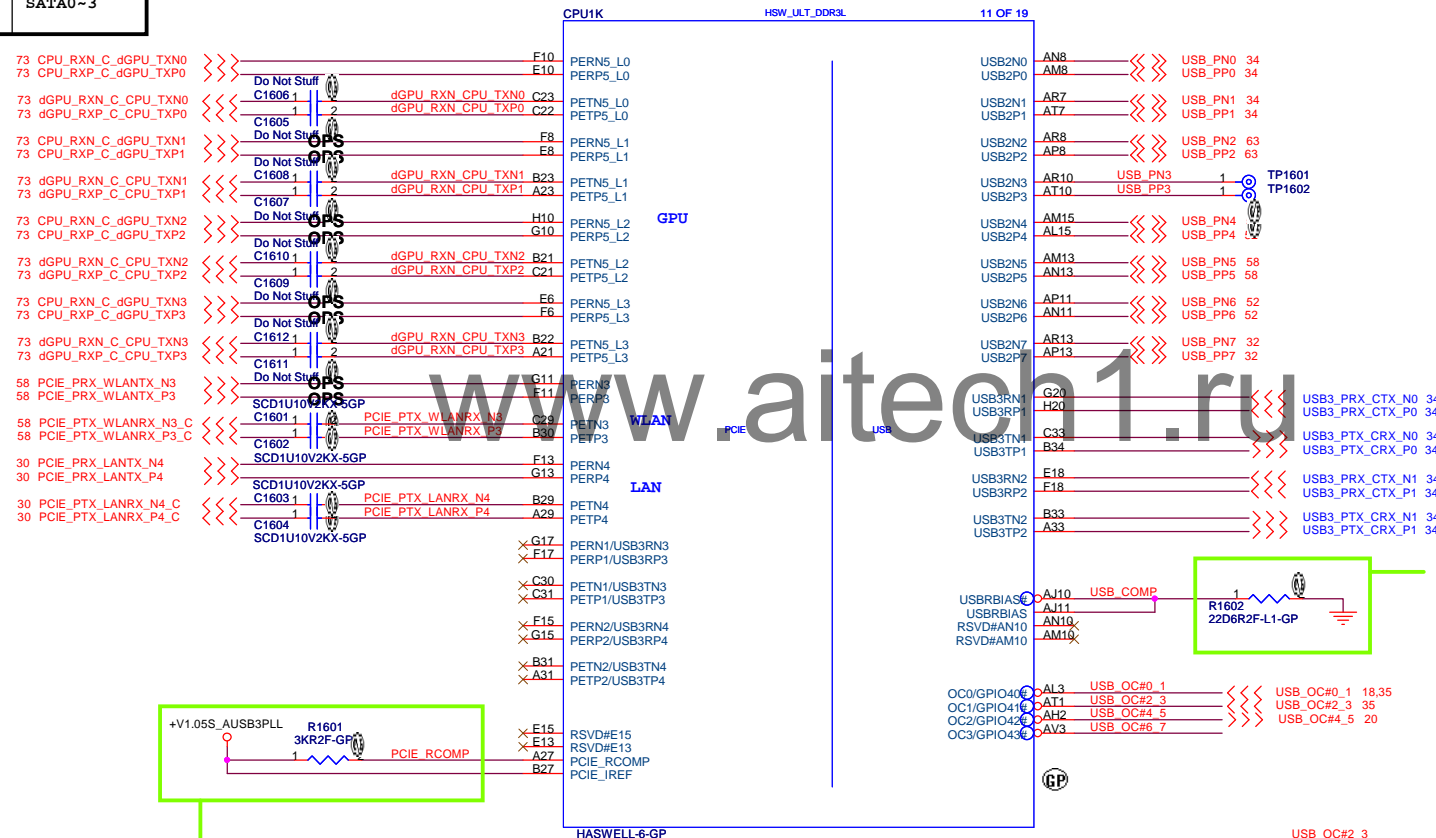
SSID = PCH

## PCIE Table

| Port     | Device | Share BUS |
|----------|--------|-----------|
| 1        | TBD    | USB3.0_3  |
| 2        | TBD    | USB3.0_4  |
| 3        | WLAN   |           |
| 4        | LAN    |           |
| 5(4lane) | GPU    |           |
| 6(4lane) | TBD    | SATA0~3   |

## USB 2.0 Table

| Pair | Device       |
|------|--------------|
| 0    | USB3.0 port1 |
| 1    | USB3.0 Port2 |
| 2    | USB2.0 Port3 |
| 3    | TBD          |
| 4    | CAMERA       |
| 5    | WLAN         |
| 6    | Touch Panel  |
| 7    | Card Reader  |



### Layout Note:

1. PCIE\_RCOMP/ PCIE\_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

### Layout Note:

1. USB\_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

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Title

**PCH (PCIE/USB)**

Size

A3

Document Number

**Latitude300 Haswell**

Rev

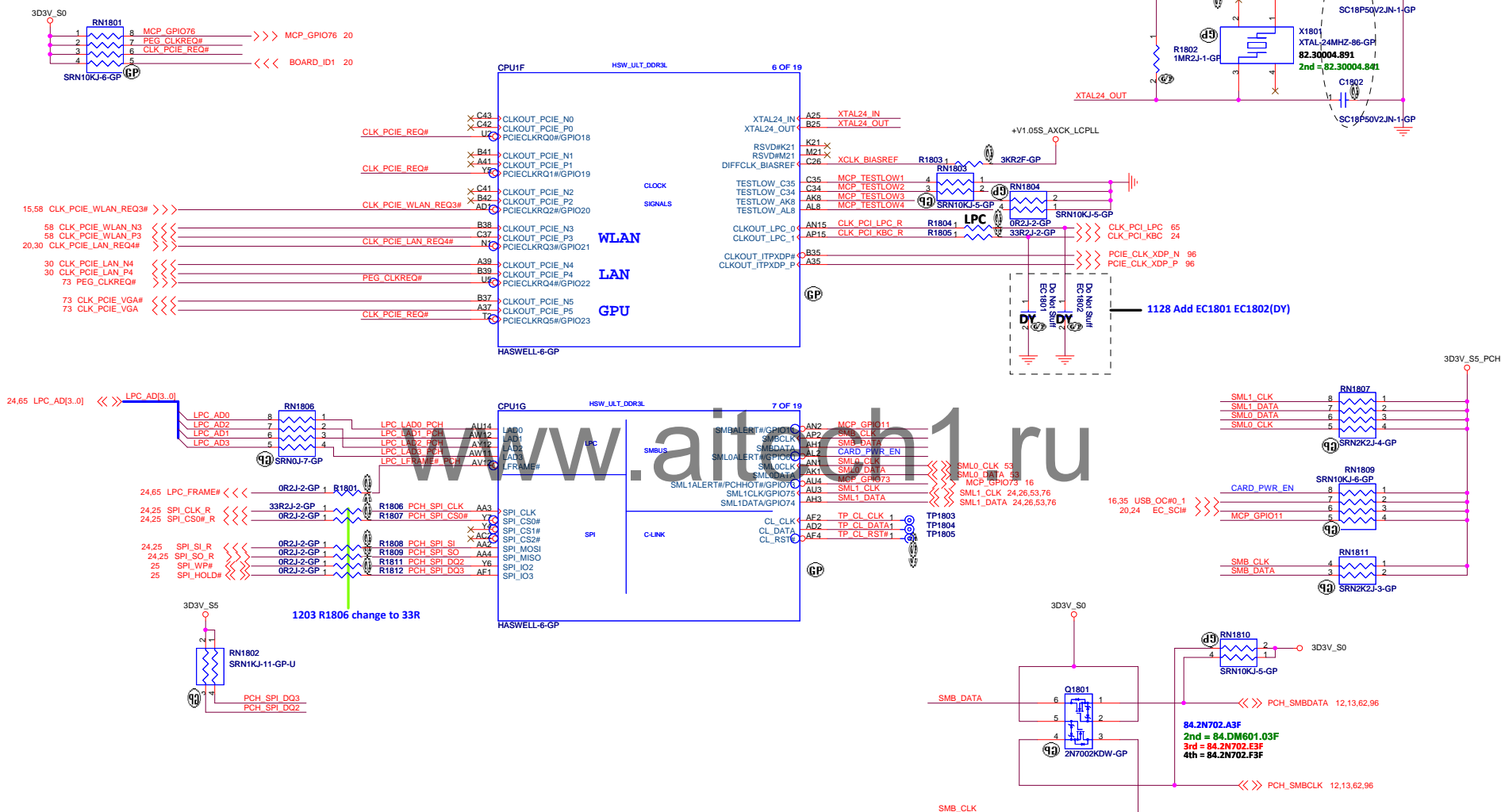
**X00**

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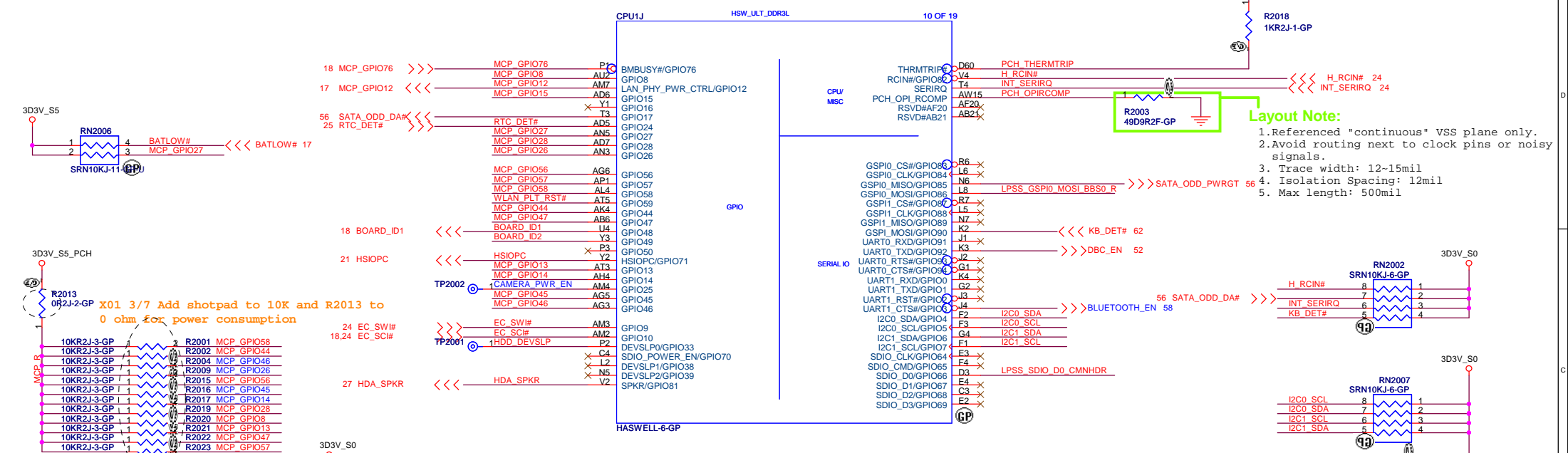


**SSID = PCH**





SSID = CPU



**Layout Note:**

- 1. Referenced "continuous" VSS plane only.
- 2. Avoid routing next to clock pins or noisy signals.
- 3. Trace width: 12~15mil
- 4. Isolation Spacing: 12mil
- 5. Max length: 500mil

**PCH strap pin:**

|          |  |
|----------|--|
| 18,30    | NO REBOOT                                  |
| HDA_SPKR | * Low = Disable (Default)<br>High = Enable |

The internal pull-down is disabled after PLTRST# deasserts

**Top-Block Swap Override mode**

|                  |  |
|------------------|--|
| SDIO_D0 / GPIO66 | High = Enable "Top-Block swap" mode (Default)<br>* Low = Disable "Top-Block swap" mode |
|------------------|--|

The internal pull-down is disabled after PLTRST# deasserts

**TLS Confidentiality**

|        |  |
|--------|--|
| GPIO15 | * Low = Disable Intel ME Crypto TLS<br>High = Enable Intel ME Crypto TLS |
|--------|--|

The internal pull-down is disabled after RSMRST# deasserts.

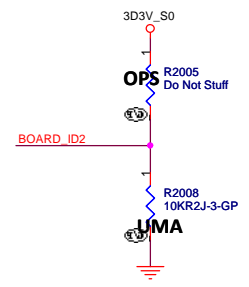
**Boot BIOS Strap Bit BBS**

|                       |                           |
|-----------------------|---------------------------|
| Boot BIOS Destination | * Low = SPI<br>High = LPC |
|-----------------------|---------------------------|

The internal pull-down is disabled after PLTRST# deasserts

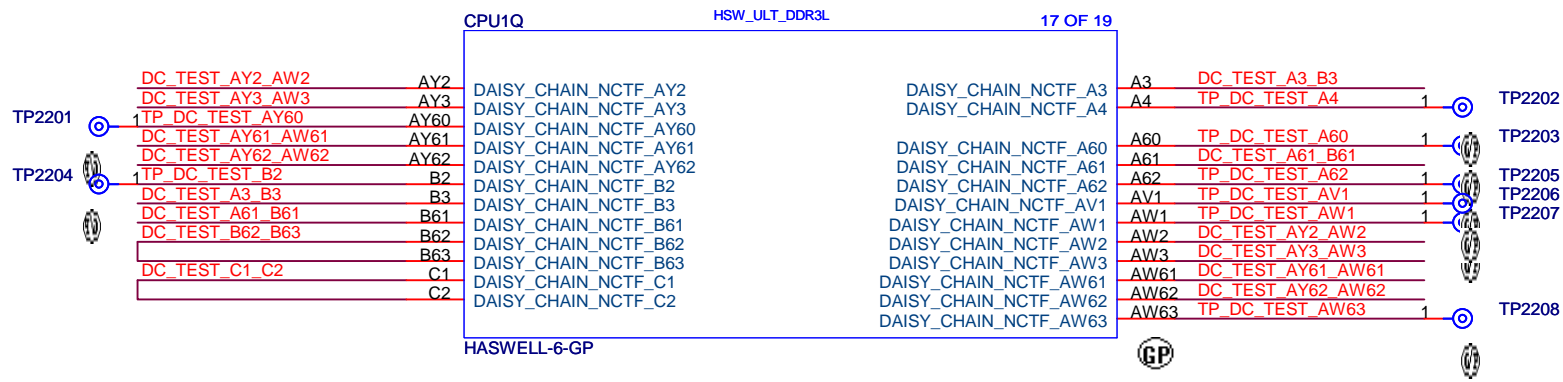
**BIOS strap pin:**

| BIOS UMA/DIS Strap pin |           |           |
|------------------------|-----------|-----------|
|                        | BOARD_ID1 | BOARD_ID2 |
| UMA                    | 1         | 0         |
| DIS                    | 1         | 1         |





SSID = PCH



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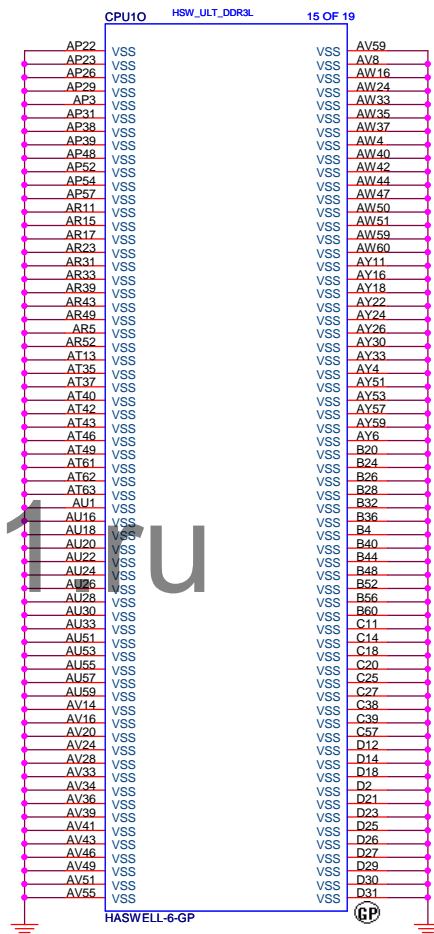
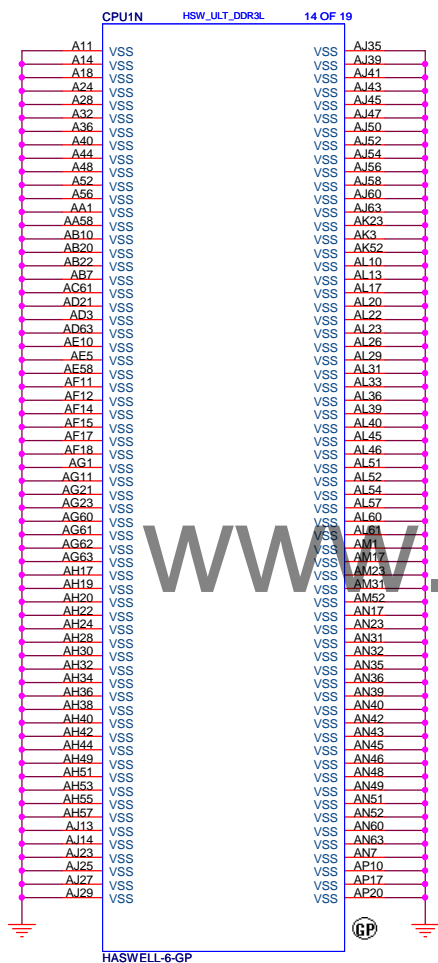
Title

(Reserved)

|            |   |                   |
|------------|---|-------------------|
| Size<br>A4 | Document Number<br><b>Latitude300 Haswell</b> | Rev<br><b>X00</b> |
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SSID = PCH



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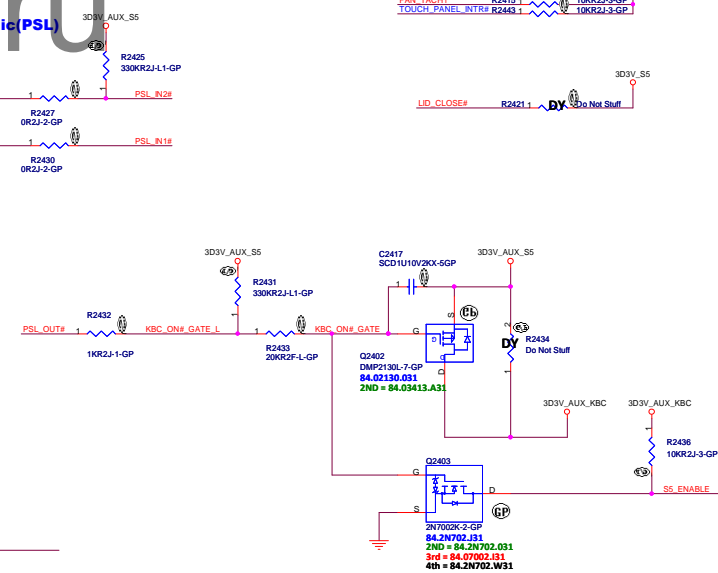
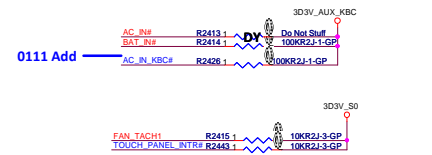
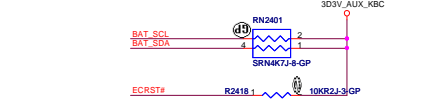
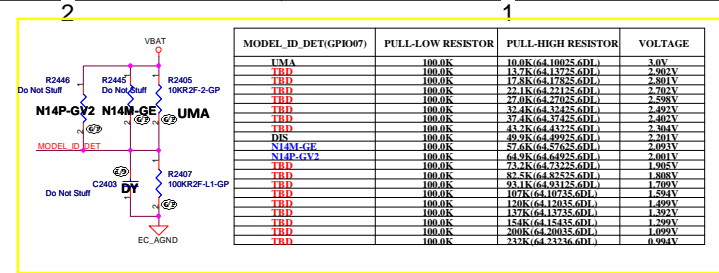
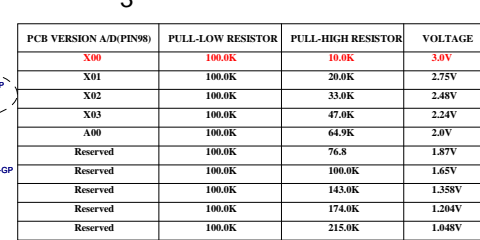
**Latitude300 Haswell**

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X00

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A

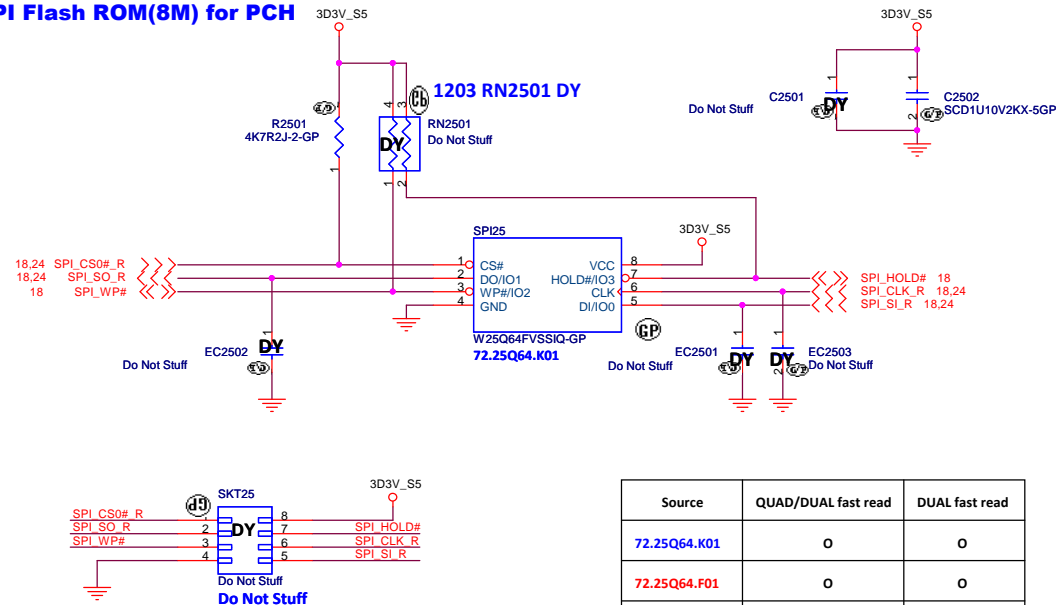


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|                     |                        |             |     |
|---------------------|------------------------|-------------|-----|
| Title               |                        |             |     |
| KBC Nuvoton NPCE885 |                        |             |     |
| Size<br>A2          | Document Number        | Rev         |     |
| Latitude300 Haswell |                        | X000        |     |
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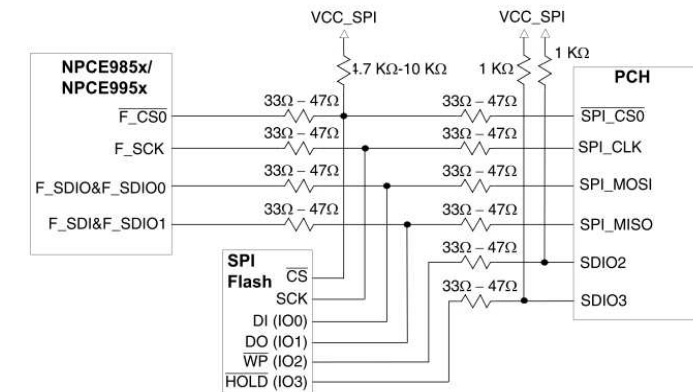
```
SSID = Flash.ROM
```

### SPI Flash ROM(8M) for PCH



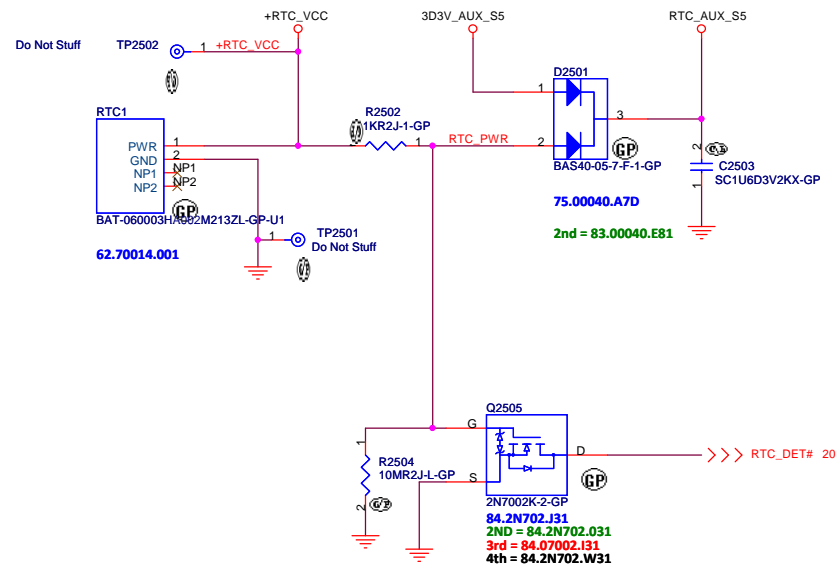
| Source       | QUAD/DUAL fast read | DUAL fast read |
|--------------|---------------------|----------------|
| 72.25Q64.K01 | 0                   | 0              |
| 72.25Q64.F01 | 0                   | 0              |
| 72.25Q64.D01 | 0                   | 0              |

### Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

**SSID = RBATT**



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Title

**Flash/RTC**

Size

| Document Number |
|-----------------|
|-----------------|

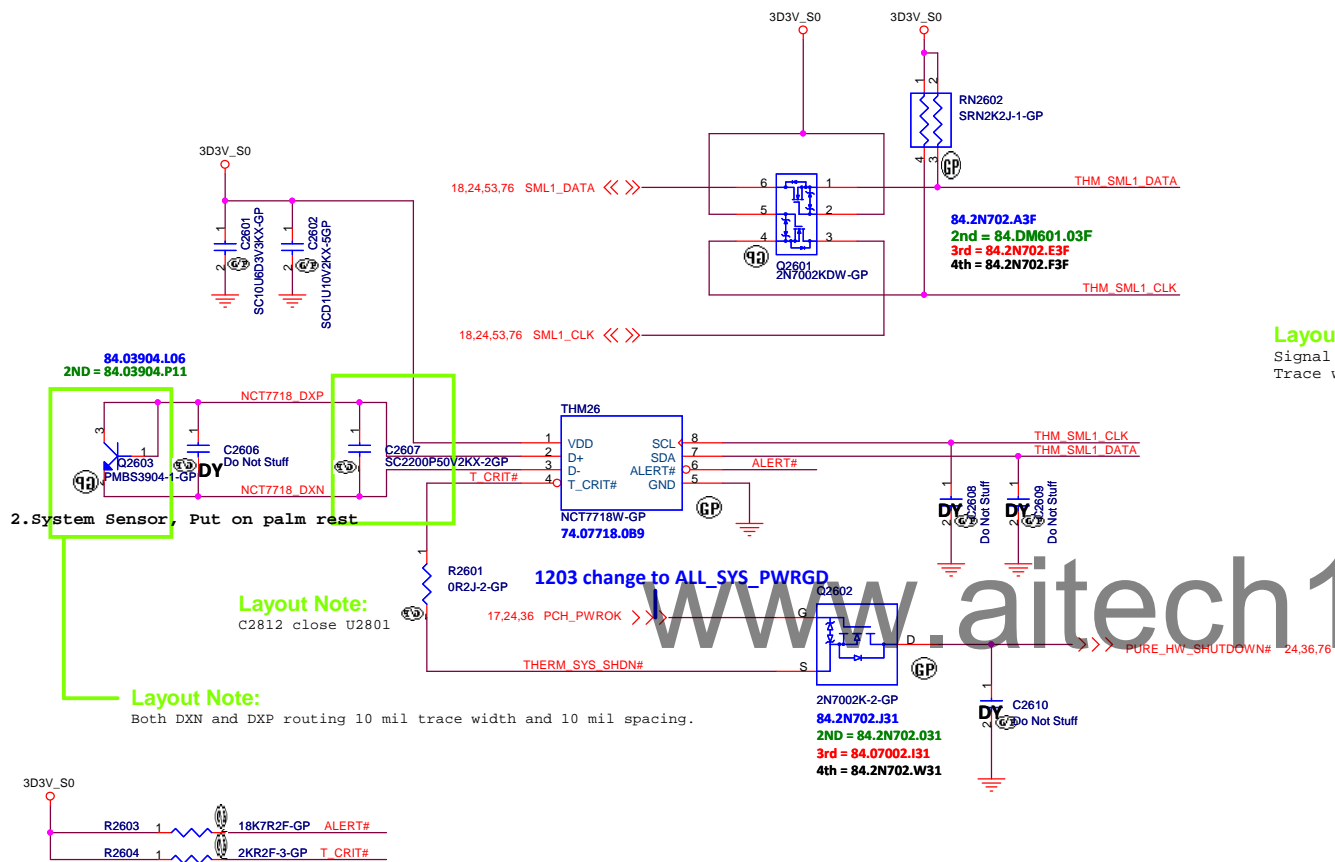
**Latitude300 Haswell**

|     |  |
|-----|--|
| Rev |  |
|-----|--|

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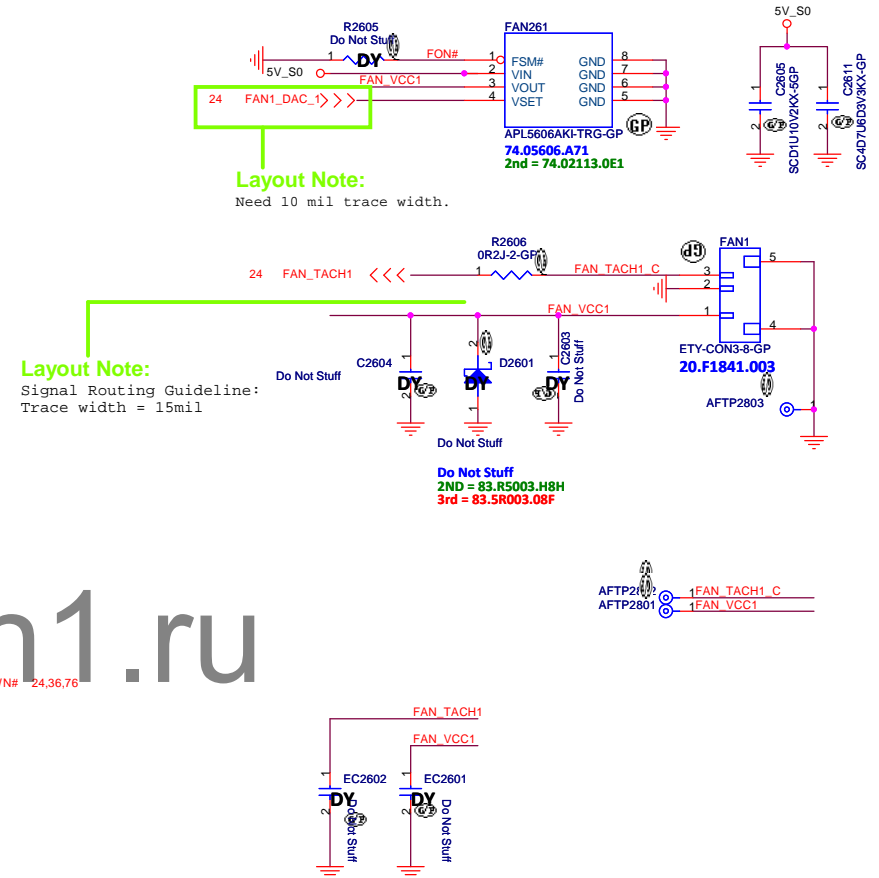
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SSID = Thermal

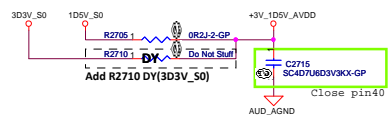
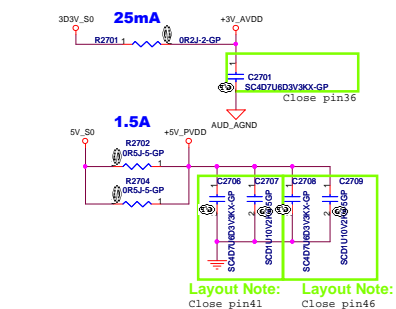
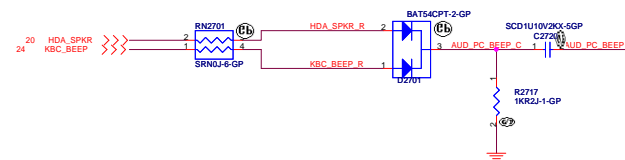
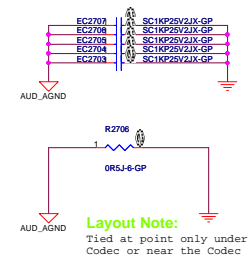
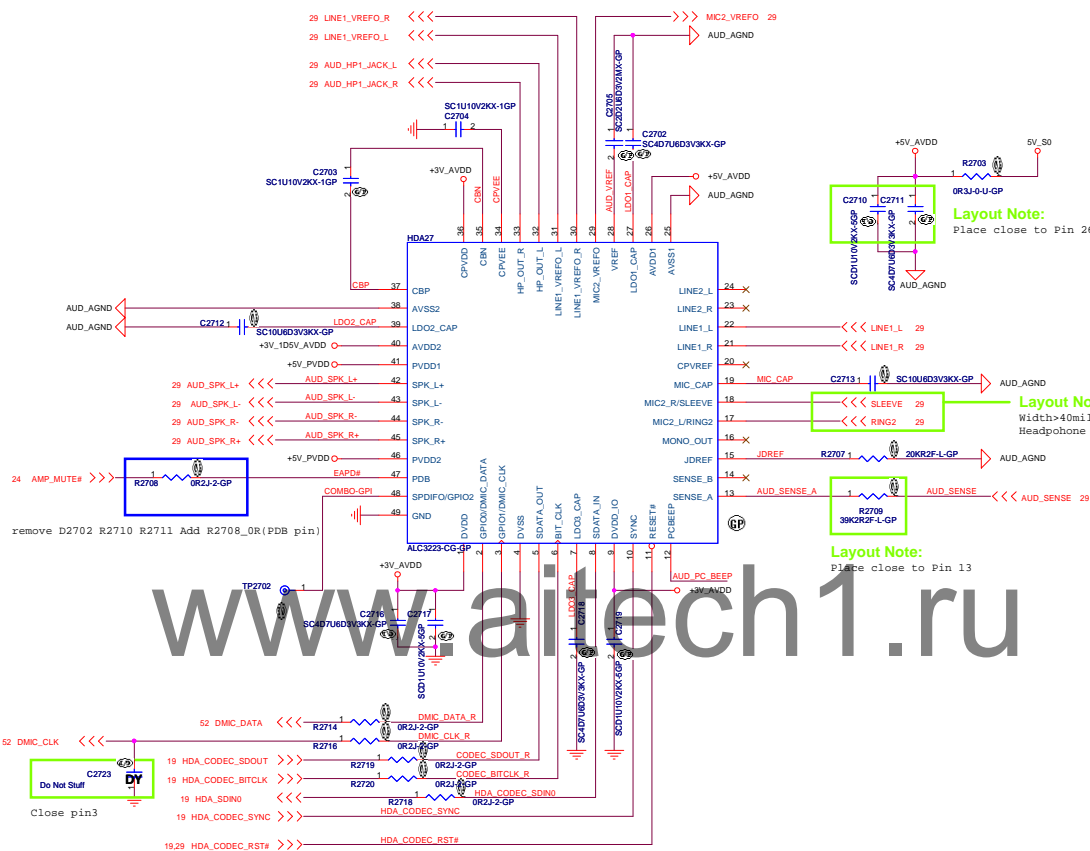
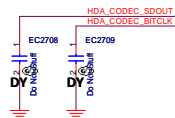


| TEMPERATURE (°C) |        | T_CRIT# |       |        |      |        |
|------------------|--------|---------|-------|--------|------|--------|
|                  |        | 2KΩ     | 7.5KΩ | 10.5KΩ | 14KΩ | 18.7KΩ |
| ALERT#           | 2KΩ    | 77      | 87    | 97     | 107  | 117    |
|                  | 7.5KΩ  | 79      | 89    | 99     | 109  | 119    |
|                  | 10.5KΩ | 81      | 91    | 101    | 111  | 121    |
|                  | 14KΩ   | 83      | 93    | 103    | 113  | 123    |
|                  | 18.7KΩ | 85      | 95    | 105    | 115  | 125    |

## Fan controller1




SSID = AUDIO

**Azalia I/F EMI**

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Title

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Document Number  
**Latitude300 Haswell**

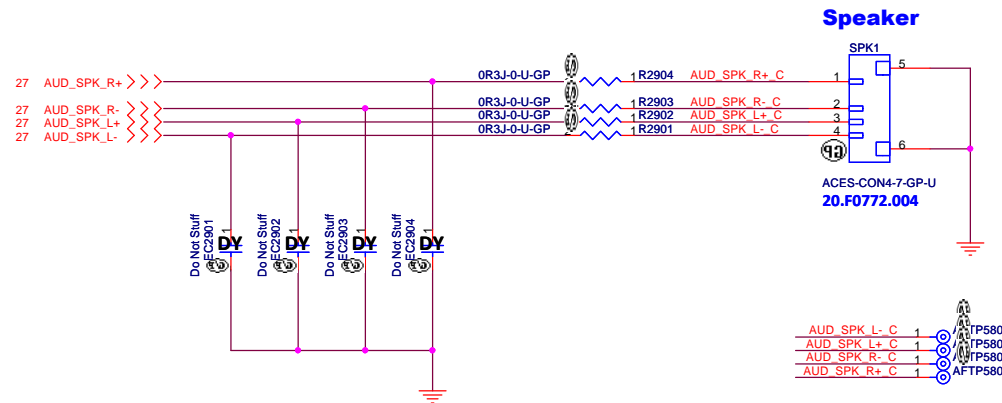
Rev  
**X00**

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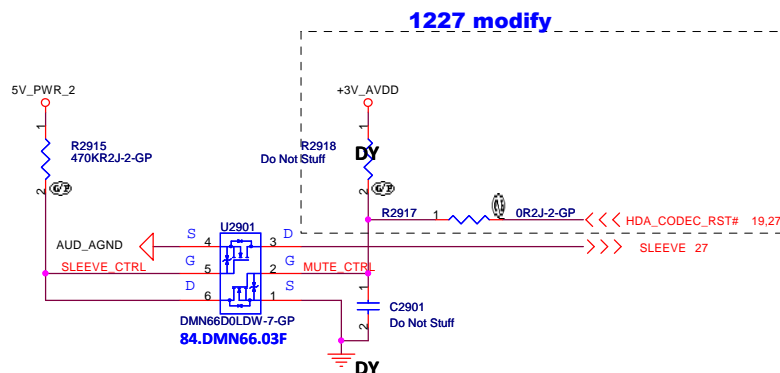
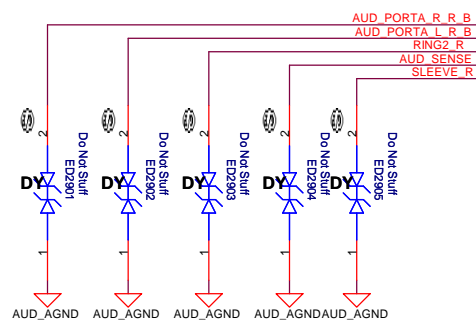
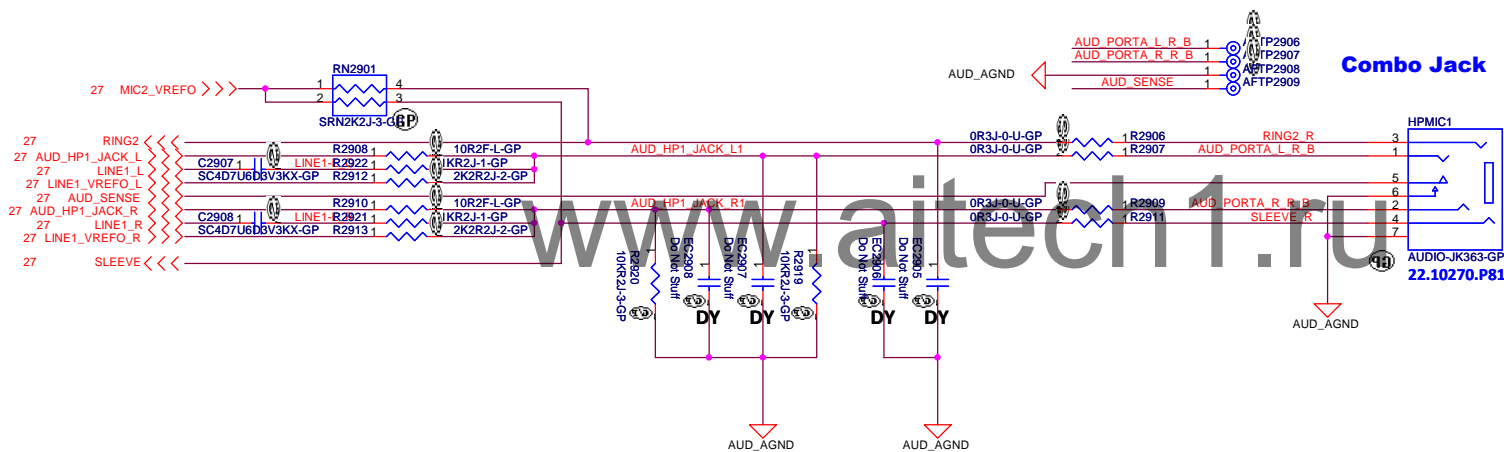
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**Reserved**

SSID = AUDIO

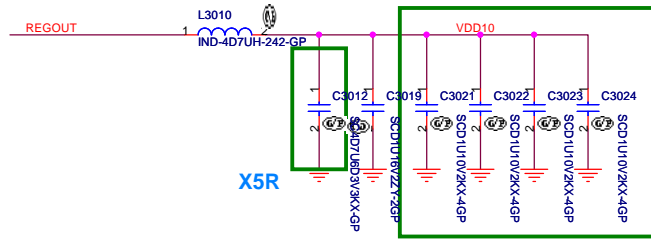


| CONN Pin | Net name |
|----------|----------|
| Pin1     | SPK_R+   |
| Pin2     | SPK_R-   |
| Pin3     | SPK_L+   |
| Pin4     | SPK_L-   |

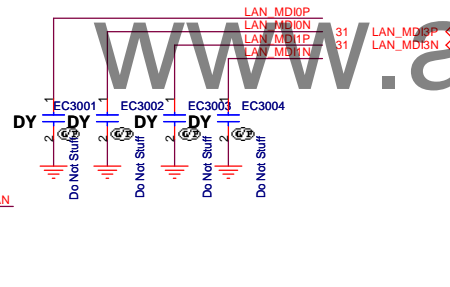
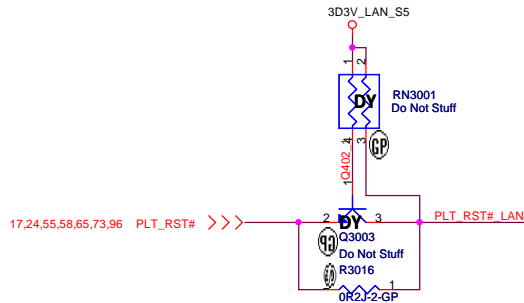
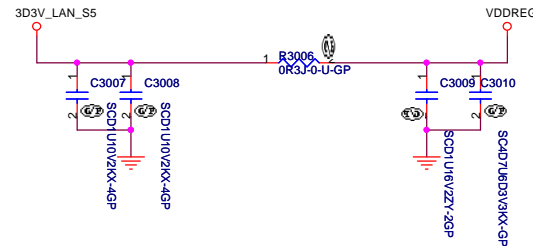


# LAN CHIP

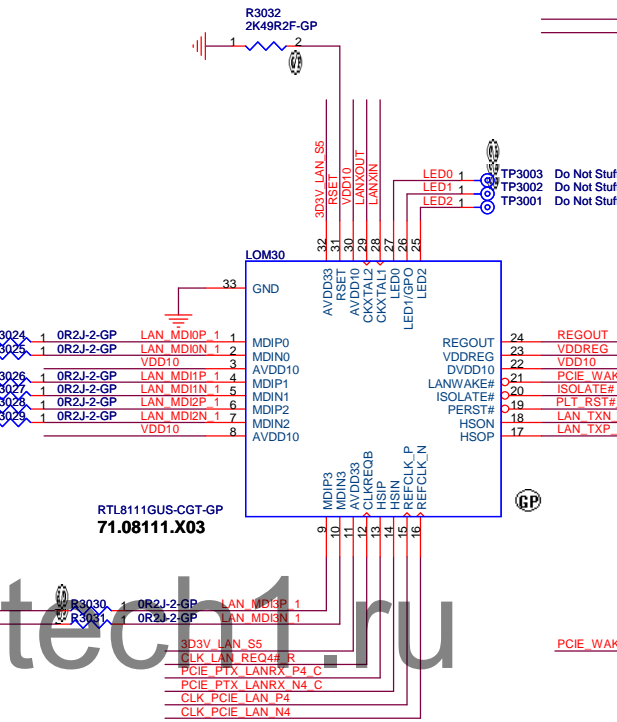
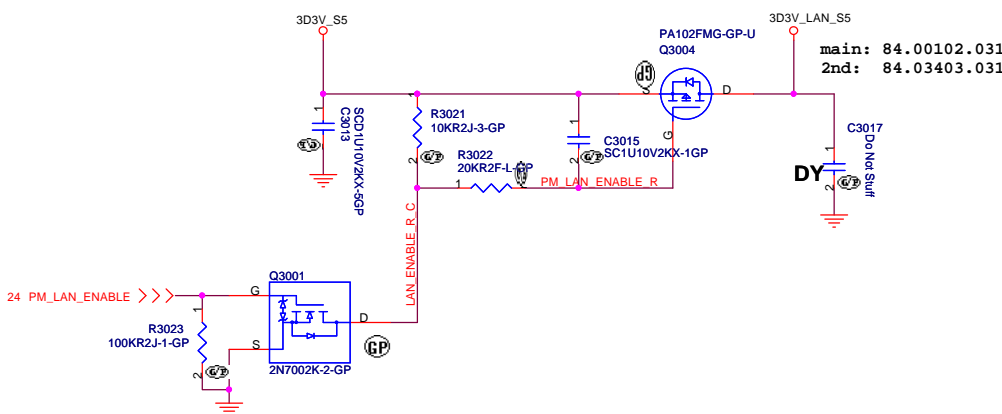
10/100 Need Only need C3021, C3022, C3023, C3024 in Pin3, 8, 22, 30



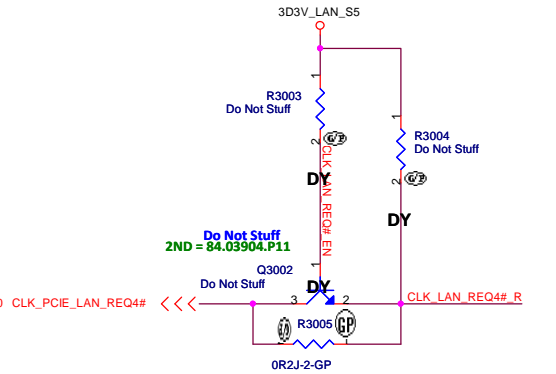
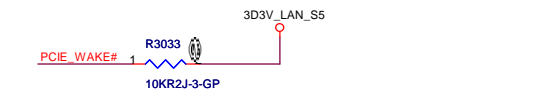
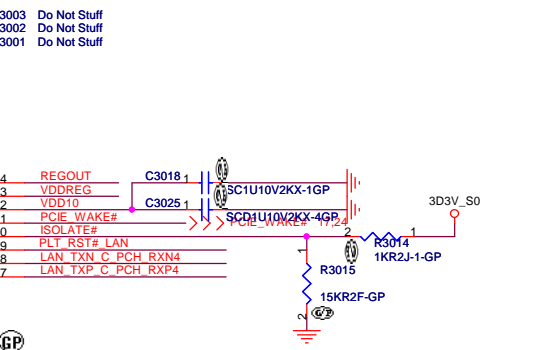
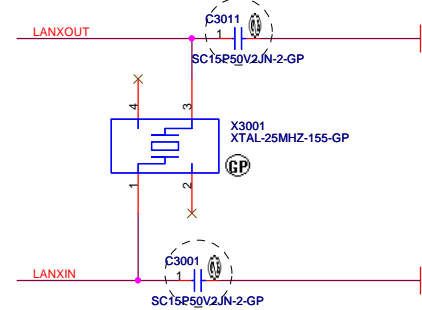
40 mils



251mA

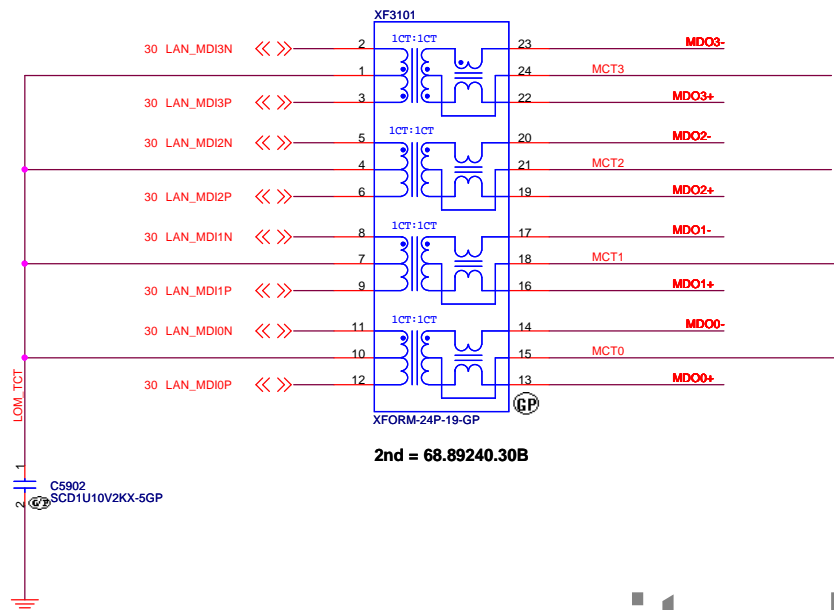


X00 3/7 Change value from test report

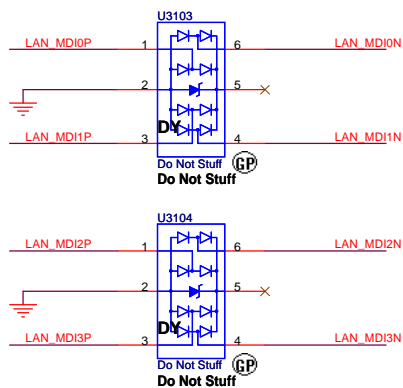


SSID = LOM

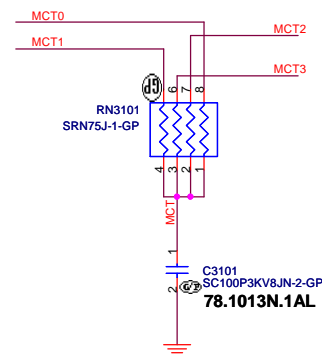
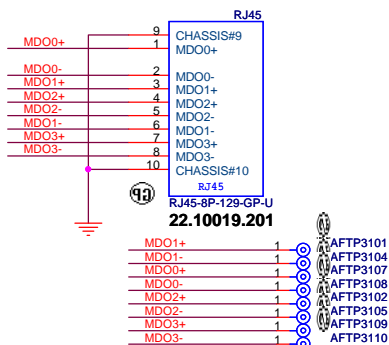
## 100/GIGA LAN TransFormer



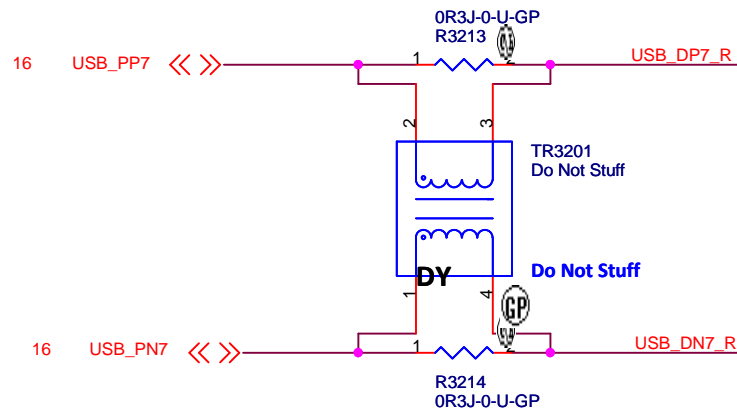
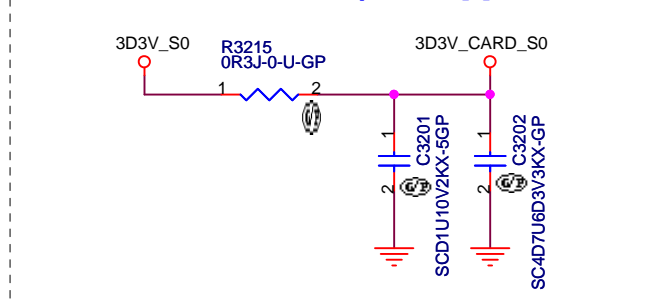
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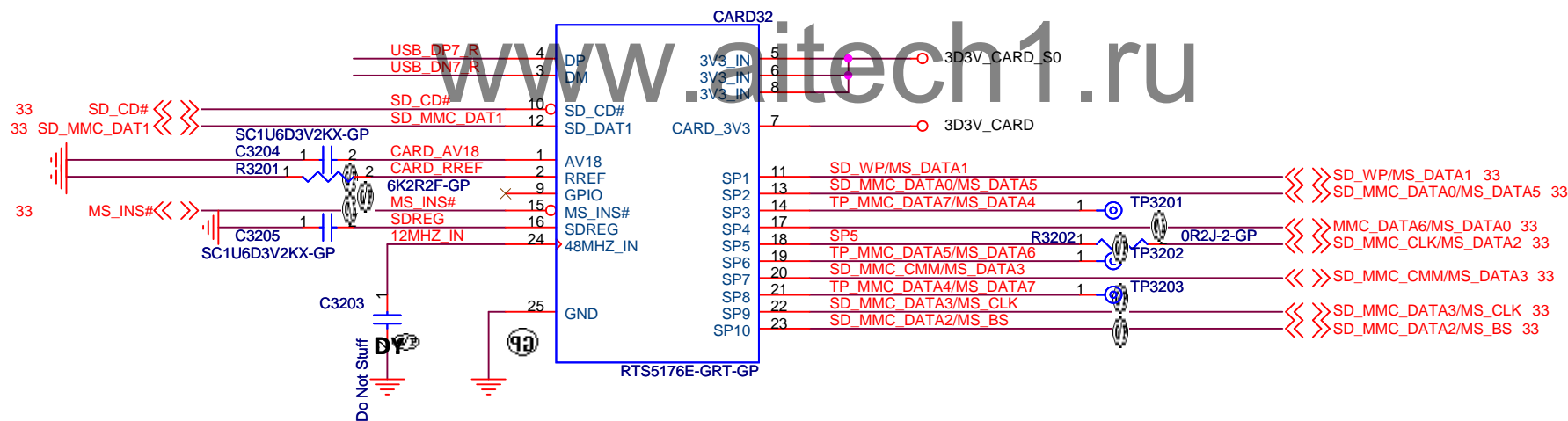
## RJ45 CONN




## 1121 remove Switch(No support D3 cold)



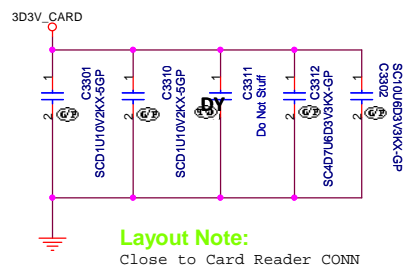
| Pin name | Net name                |
|----------|-------------------------|
| SD_DAT1  | SD_MMC_DAT1             |
| SP1      | SD_WP/MS_DATA1          |
| SP2      | SD_MMC_DATA0/MS_DATA5   |
| SP3      | MMC_DATA7/MS_DATA4      |
| SP4      | MMC_DATA6/MS_DATA0      |
| SP5      | SD_MMC_CLK/MS_DATA2     |
| SP6      | MMC_DATA5/MS_DATA6      |
| SP7      | SD_MMC Command/MS_DATA3 |
| SP8      | MMC_DATA4/MS_DATA7      |
| SP9      | SD_MMC_DATA3/MS_CLK     |
| SP10     | SD_MMC_DATA2/MS_BS      |



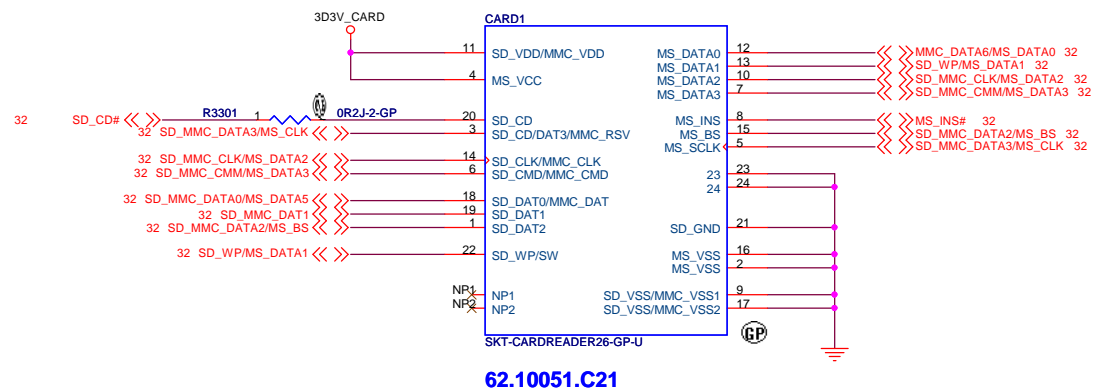
UM

|   |                 |  |            |
|---|-----------------|--|------------|
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|   |                 | <b>Card Reader-RTS5176</b><br><b>Latitude300 Haswell</b> |            |
| Size<br>A4  | Document Number | Date: Friday, March 15, 2013                             | Rev<br>X00 |
| Sheet 32 of 104   |                 |  |            |

SSID = SDIO

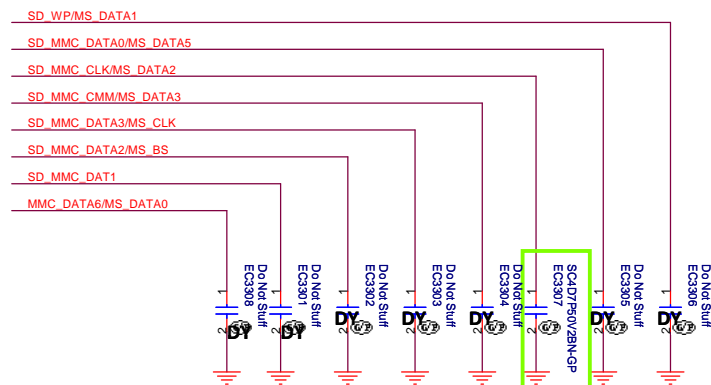


SD/MS/MMC Card Connector



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For EMI Reserved



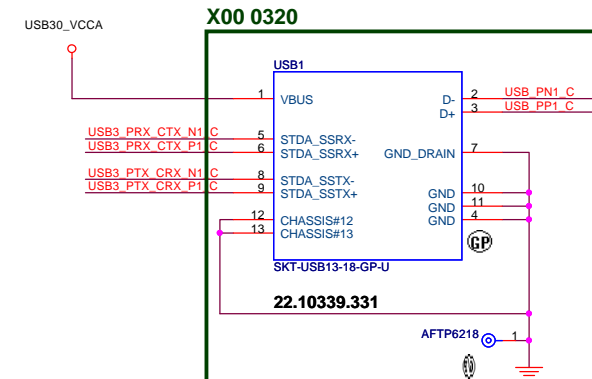
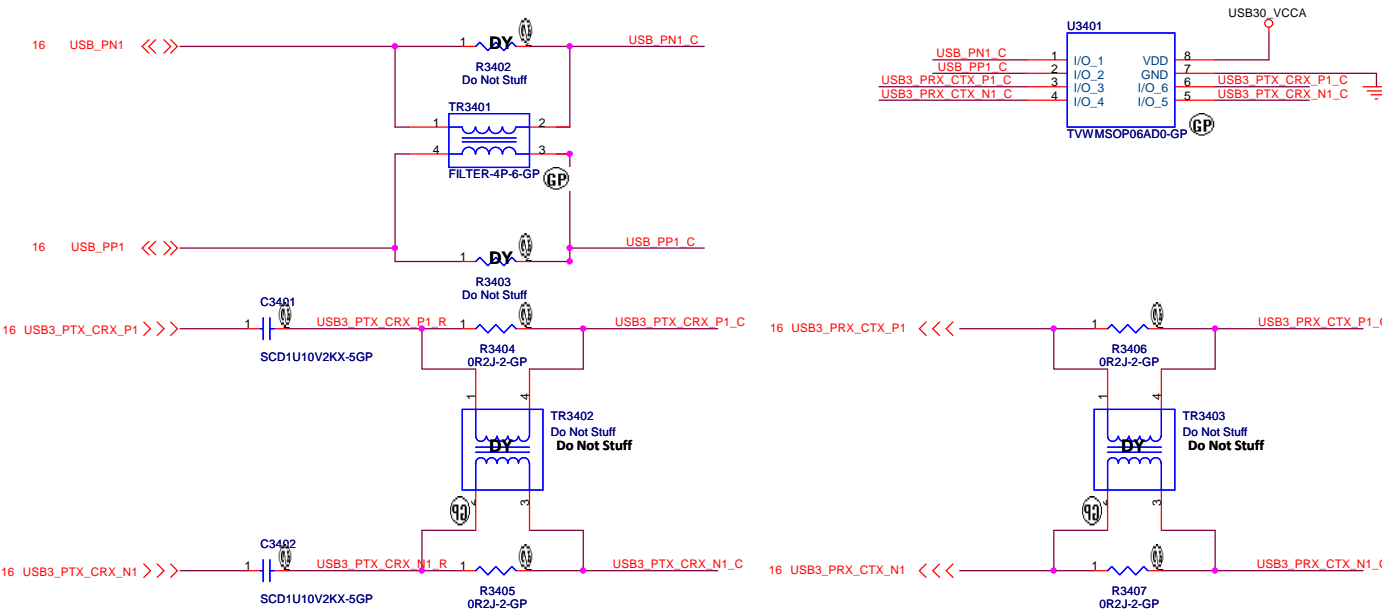
Layout Note:  
please close U3201

1203 modify 10P change to 4.7P

SSID = USB

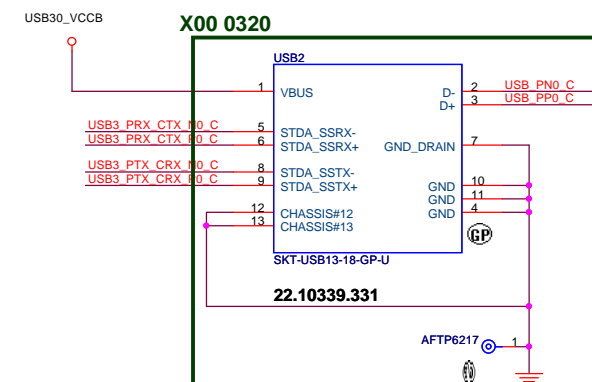
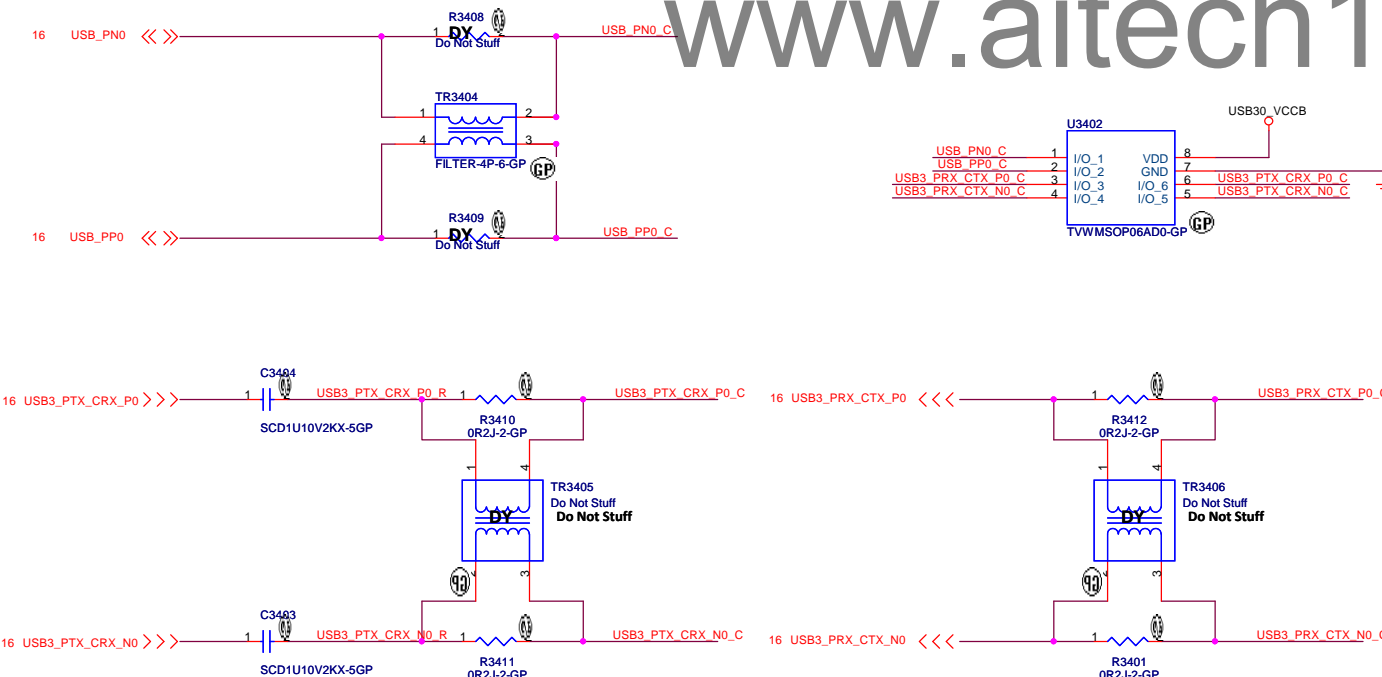
## USB3.0 Port1

USB\_PN1\_C 1  
USB30\_VCCA 1  
USB\_PP1\_C 1  
FTP6204  
FTP6205  
AFTP6209



## USB3.0 Port2

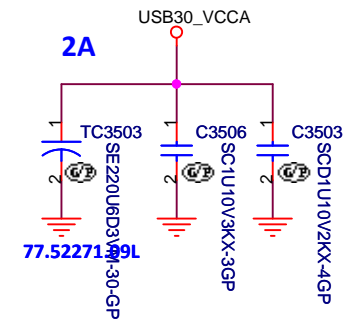
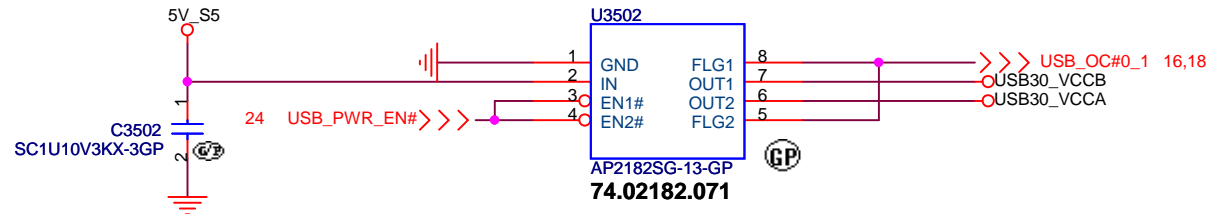
USB30\_VCCB 1  
USB\_PN0\_C 1  
USB\_PP0\_C 1  
FTP6210  
AFTP6211  
AFTP6212



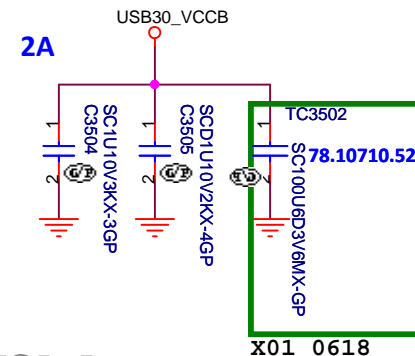
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Title  
**USB 3.0**  
Size A3 Document Number  
**Latitude300 Haswell** Rev  
**X00**  
Date: Friday, March 15, 2013 Sheet 34 of 104



**USB3.0 Port1**

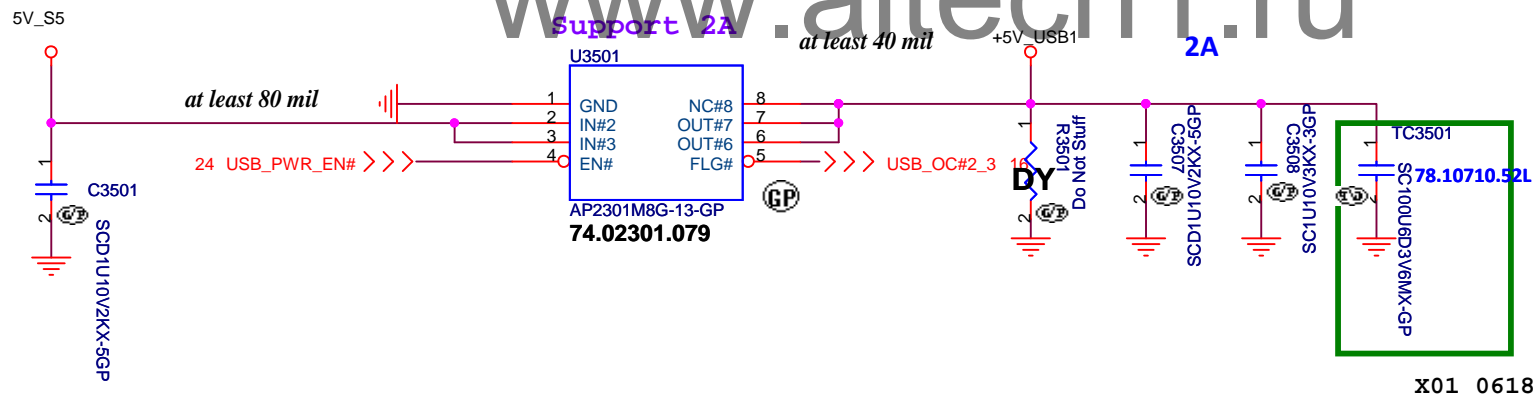


**USB3.0 Port2**

**Right USB Power x1**

Support 2A

at least 40 mil



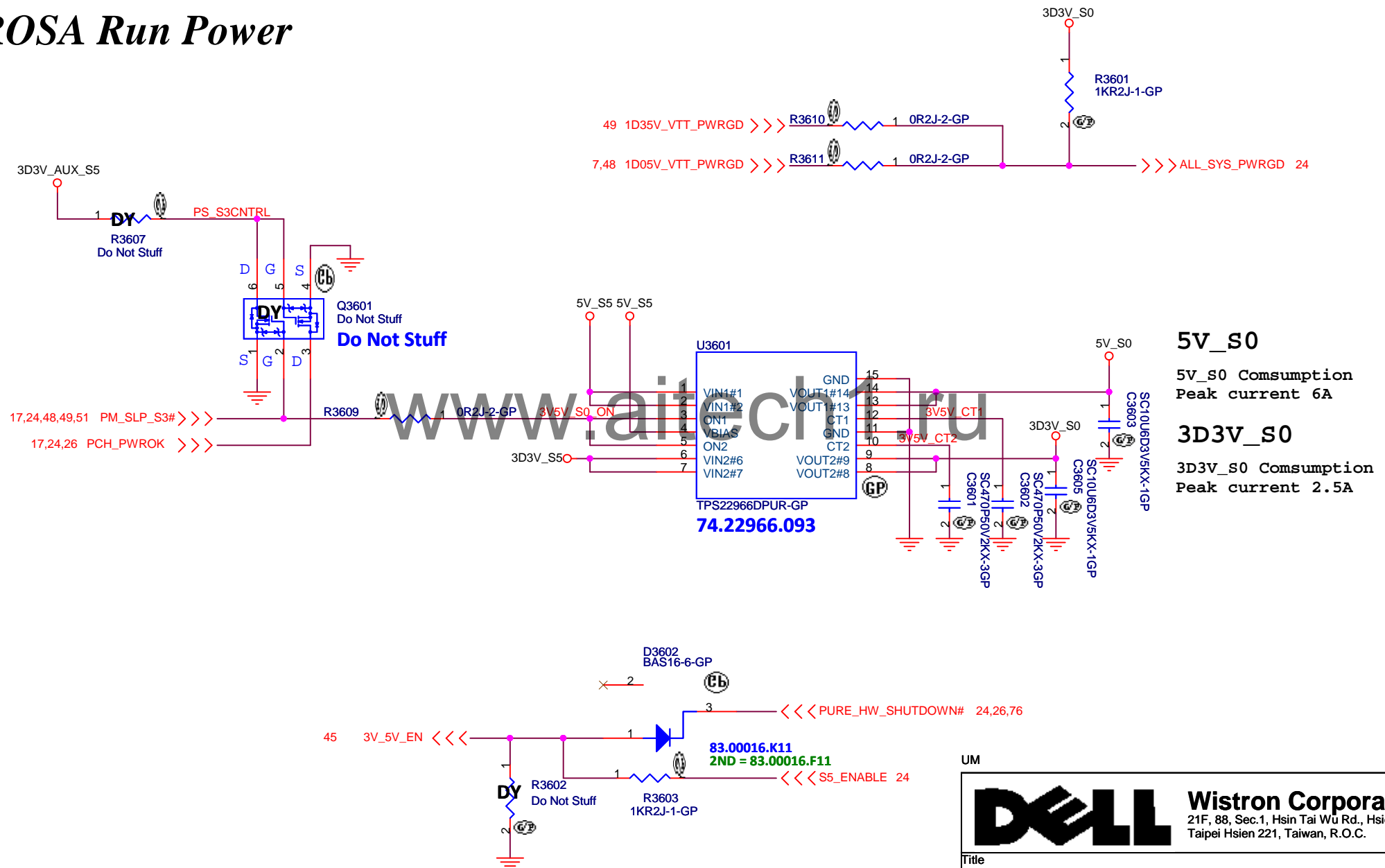
UM

|                              |   |   |                   |
|------------------------------|---|---|-------------------|
| <b>DELL</b>                  |   | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                   |
| Title<br><b>USB Power SW</b> |   |   |                   |
| Size                         | Document Number<br><b>Latitude300 Haswell</b> |   | Rev<br><b>X00</b> |
| Date: Friday, March 15, 2013 |   | Sheet 35 of 104   |                   |

```
SSID = Reset.Suspend
```

# Power Good

## ***ROSA Run Power***



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Titl

## Power Plane Enable

**Siz**

Document Number

ev

# Latitude300 Haswel

**X00**

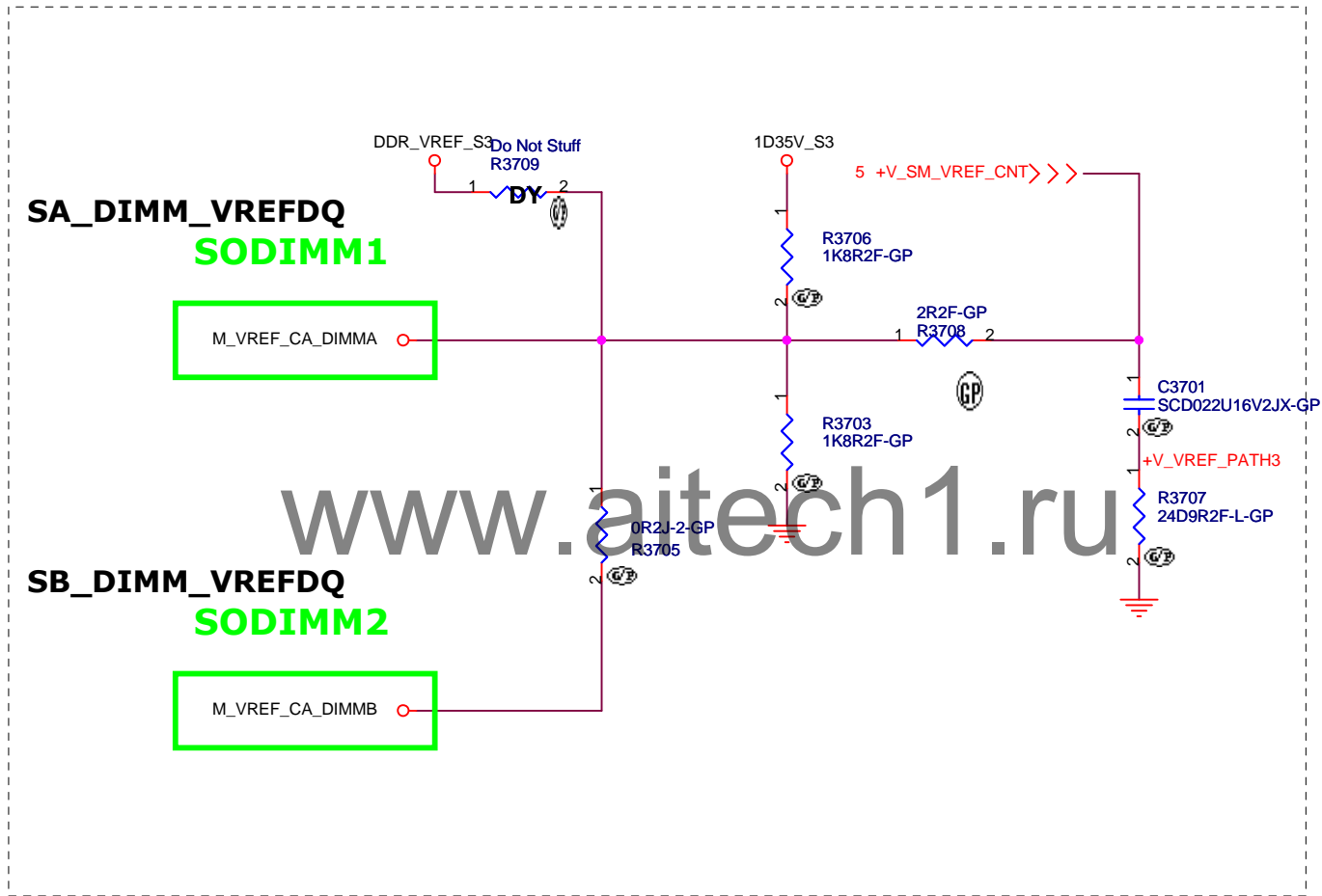
Date: Friday, March 15, 2013

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4

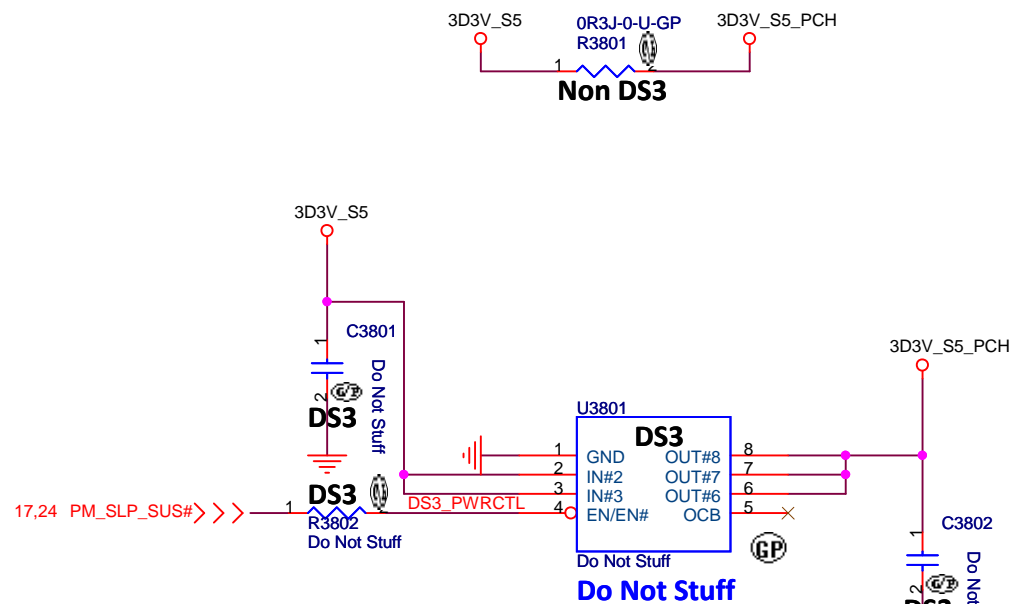
**Layout Note:**

Place Close SO-DIMM



UM

|                                      |   |   |                   |
|--------------------------------------|---|---|-------------------|
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| Title<br><b>S3 Reduction Circuit</b> |   |   |                   |
| Size<br>A4                           | Document Number<br><b>Latitude300 Haswell</b> |   | Rev<br><b>X00</b> |
| Date:<br>Friday, March 15, 2013      | Sheet<br>37                                   |   | of<br>104         |



1210 change power switch (RdsON:100m ohm)

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|                              |   |   |                   |
|------------------------------|---|---|-------------------|
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| <b>Title</b><br><b>DSW</b>   |   |   |                   |
| Size<br>A4                   | Document Number<br><b>Latitude300 Haswell</b> |   | Rev<br><b>X00</b> |
| Date: Friday, March 15, 2013 | Sheet 38                                      | of  | 104               |

SSID = CPU

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|   |                            |   |     |
|---|----------------------------|---|-----|
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| Title   |                            |   |     |
| <b>CPU (POWER1)</b>   |                            |   |     |
| Size  | Document Number            | Rev   |     |
| Custom  | <b>Latitude300 Haswell</b> | <b>X00</b>  |     |
| Date:   | Friday, March 15, 2013     | Sheet 39 of   | 104 |

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|---|---|---|-------------------|
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| Title   |   |   |                   |
| <b>Reserved</b>   |   |   |                   |
| Size<br>A3  | Document Number<br><b>Latitude300 Haswell</b> |   | Rev<br><b>X00</b> |
| Date: Friday, March 15, 2013  |   | Sheet 40 of   | 104               |

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

Document Number  
**Latitude300 Haswell**

Rev  
**X00**

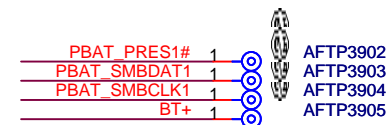
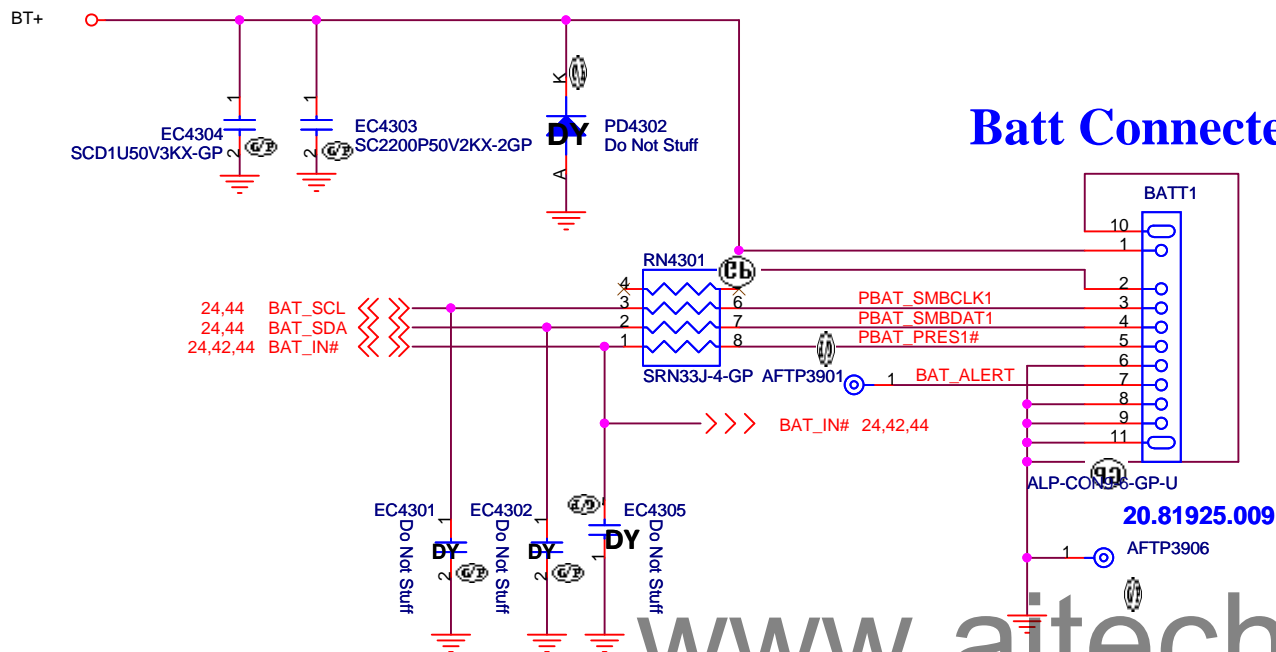
Date: Friday, March 15, 2013

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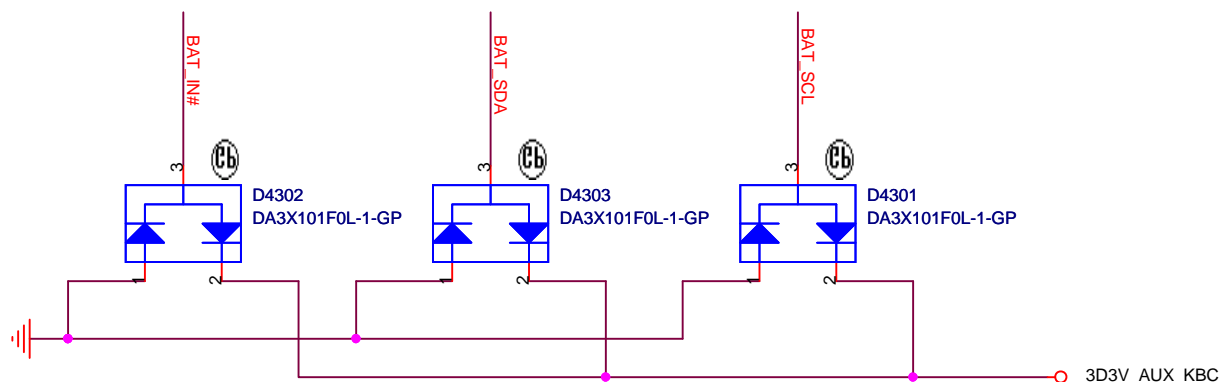
Reserved



**SSID = PWR.Support**



Placement: Close to Batt Connector



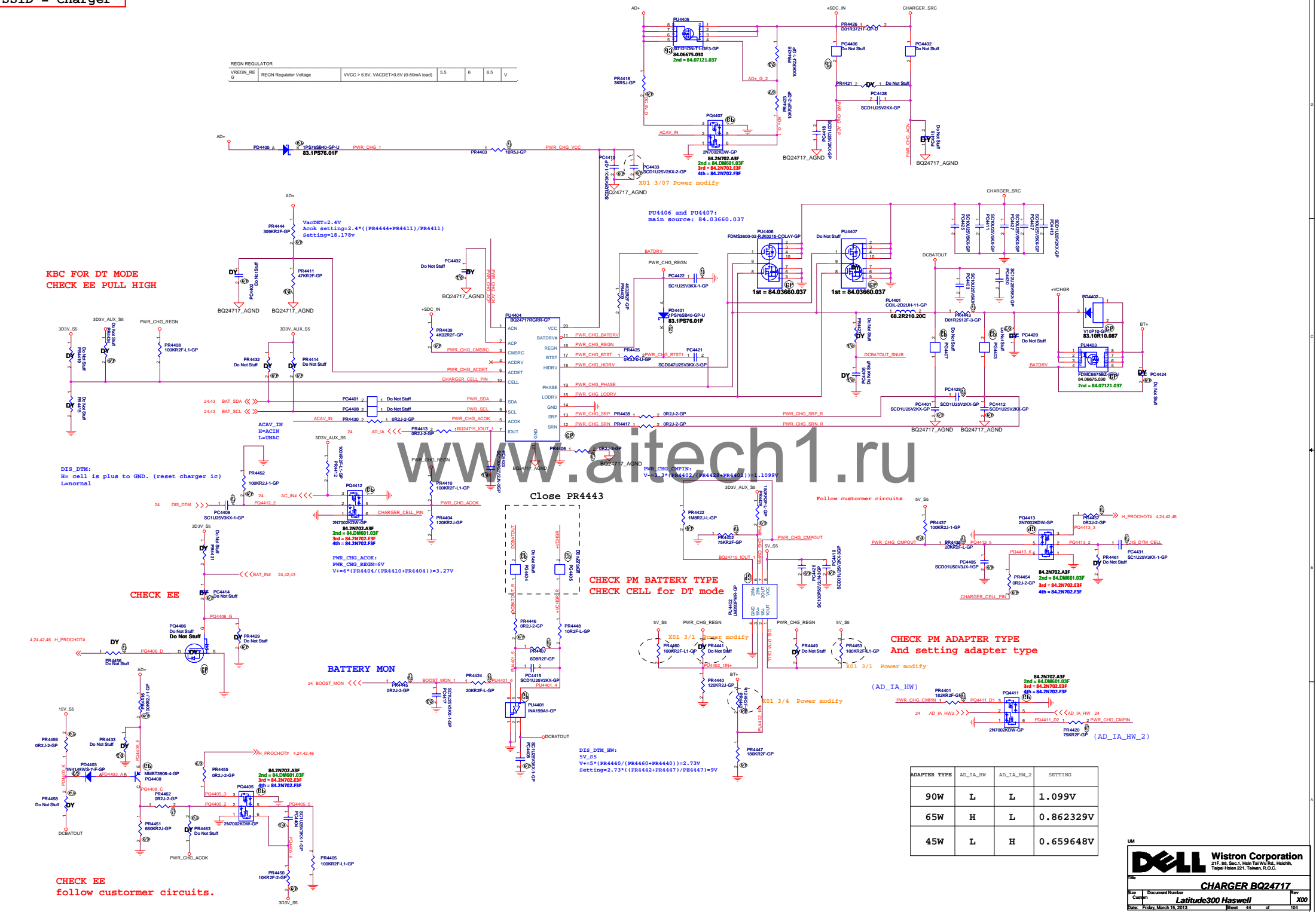
75.03101.07D  
2nd = 83.00099.K11  
3rd = 83.00099.M11

75.03101.07D  
2nd = 83.00099.K11  
3rd = 83.00099.M11

75.03101.07D  
2nd = 83.00099.K11  
3rd = 83.00099.M11

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|                              |   |  |                   |
|------------------------------|---|--|-------------------|
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| Title                        |   |  |                   |
| <b>BATT CONN</b>             |   |  |                   |
| Size<br>A4                   | Document Number<br><b>Latitude300 Haswell</b> |  | Rev<br><b>X00</b> |
| Date: Friday, March 15, 2013 | Sheet 43                                      | of   | 104               |



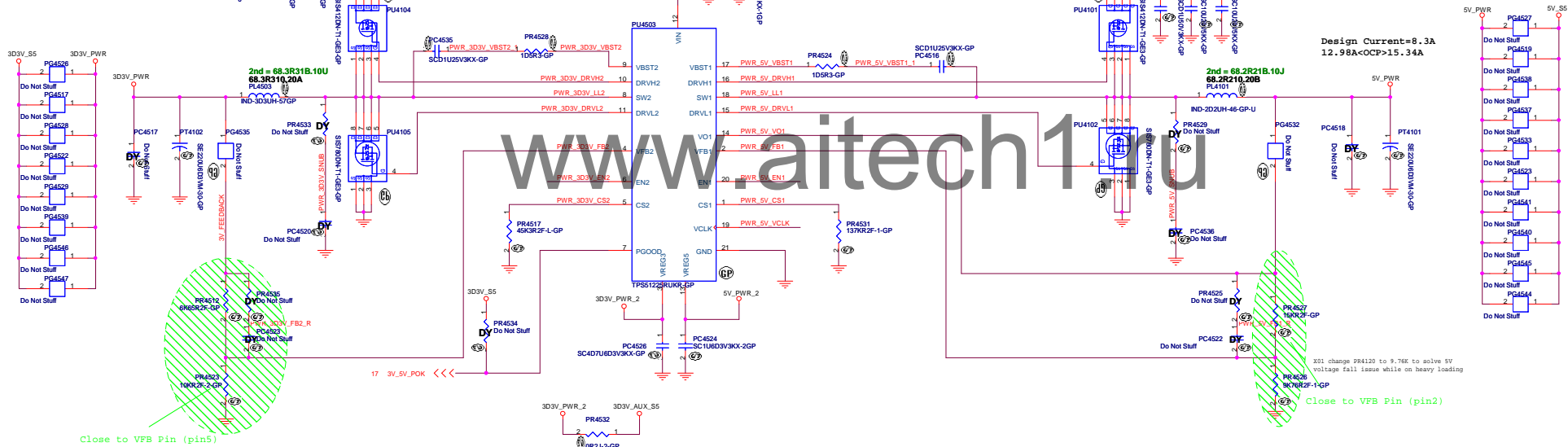
REGN REGULATOR

|          |                        |  |     |   |     |   |
|----------|------------------------|--|-----|---|-----|---|
| VREGN_RE | REGN Regulator Voltage | VVCC = 6.5V, VACDET=0.6V (0-50mA load) | 5.5 | 6 | 6.5 | V |
|----------|------------------------|--|-----|---|-----|---|

| ADAPTER TYPE | AD_IA_HW | AD_IA_HW2 | SETTING   |
|--------------|----------|-----------|-----------|
| 90W          | L        | L         | 1.099V    |
| 65W          | H        | L         | 0.862329V |
| 45W          | L        | H         | 0.659648V |

SSID = PWR.Plane.Regulator\_5v3p3v

Design Current=3.3A  
5.17A<OCP>6.11A

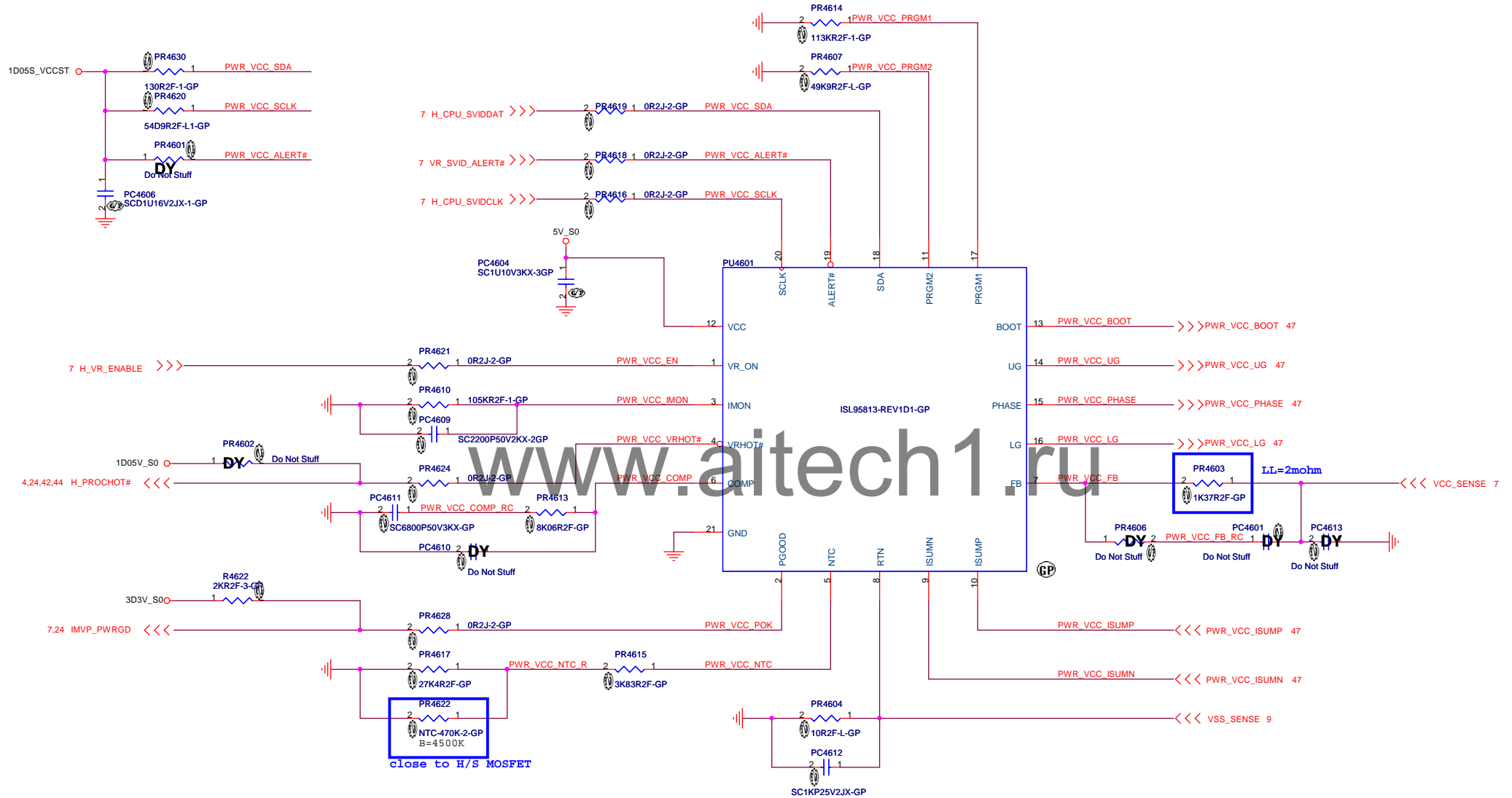


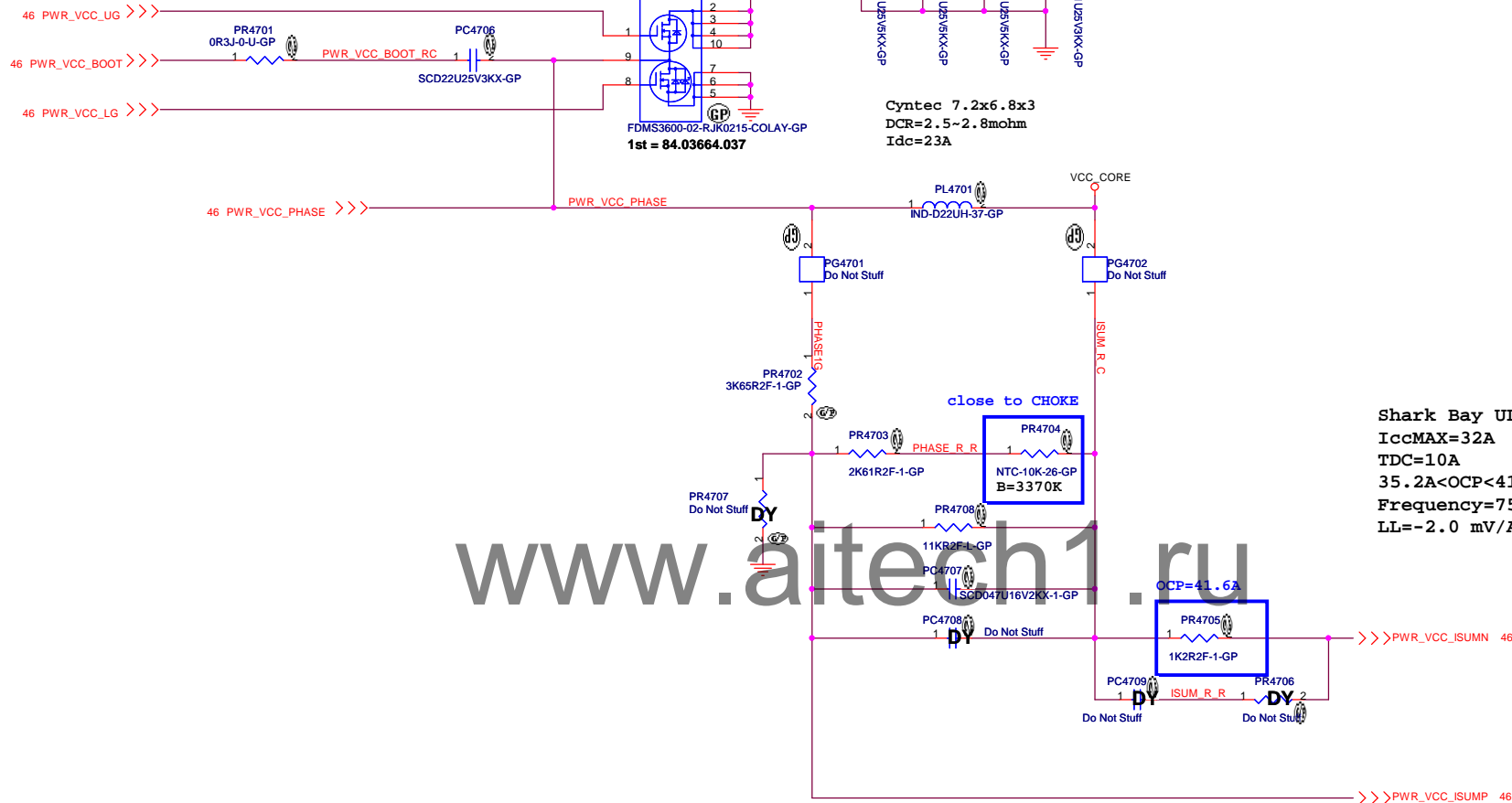
TPS51225 & TPS51285 Co-lay

|        | TPS51225 | TPS51285 |
|--------|----------|----------|
| PR4510 | 45.3KK   | 9.09K    |
| PR4511 | 110K     | 22.1K    |

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B  
O/P cap:CHIP CAP POL 220U 6.3V M 6.3\*4.5 /Matsuki/ 17mOhm / 77.52271.09L  
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

SSID = CPU.Regulator

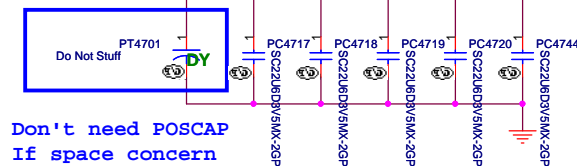




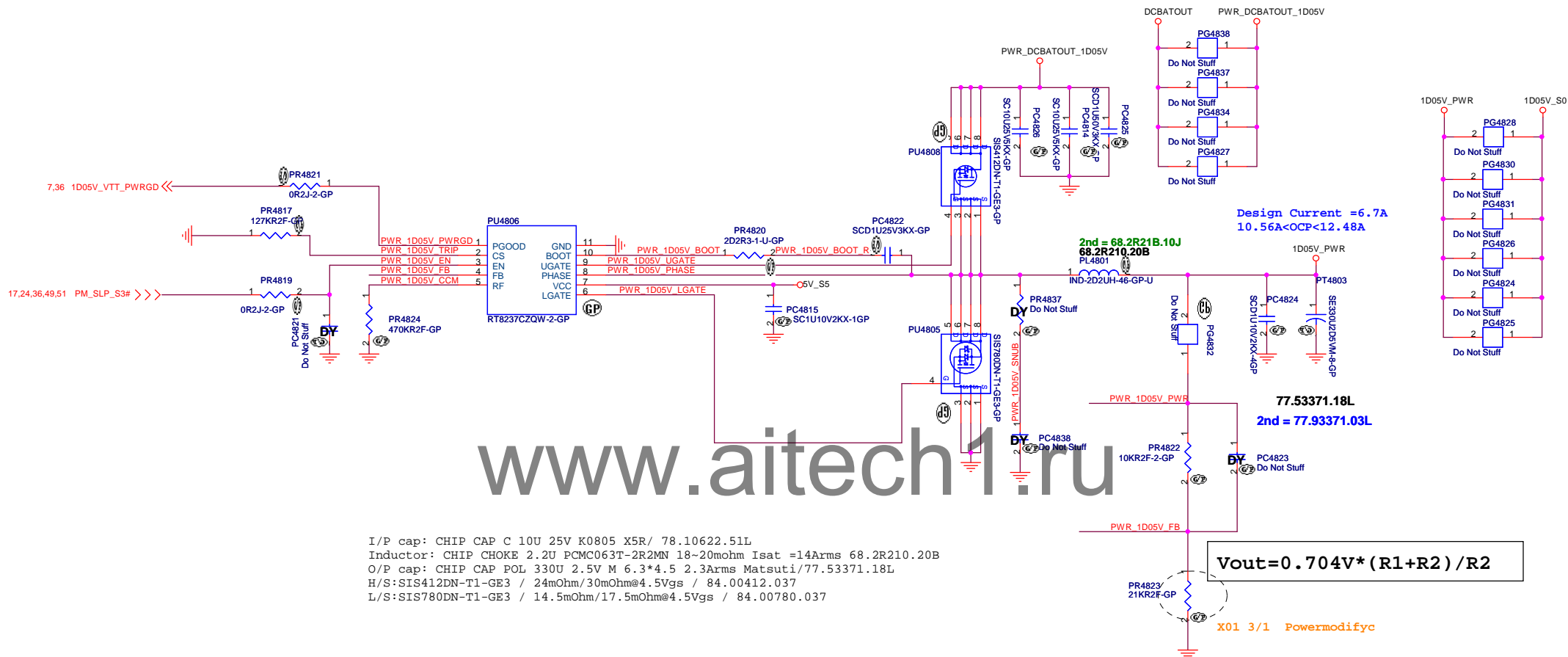
Shark Bay ULT 15W CPU  
 IccMAX=32A  
 TDC=10A  
 35.2A<OCP<41.6A  
 Frequency=750KHZ  
 LL=-2.0 mV/A

22uF/6.3V/0805\*13  
 330uF/2.5V/6.3\*4.5/12mohm\*1

X01 3/1 Power for pass transient spec



```
SSID = PWR.Plane.Regulator_1p05v
```

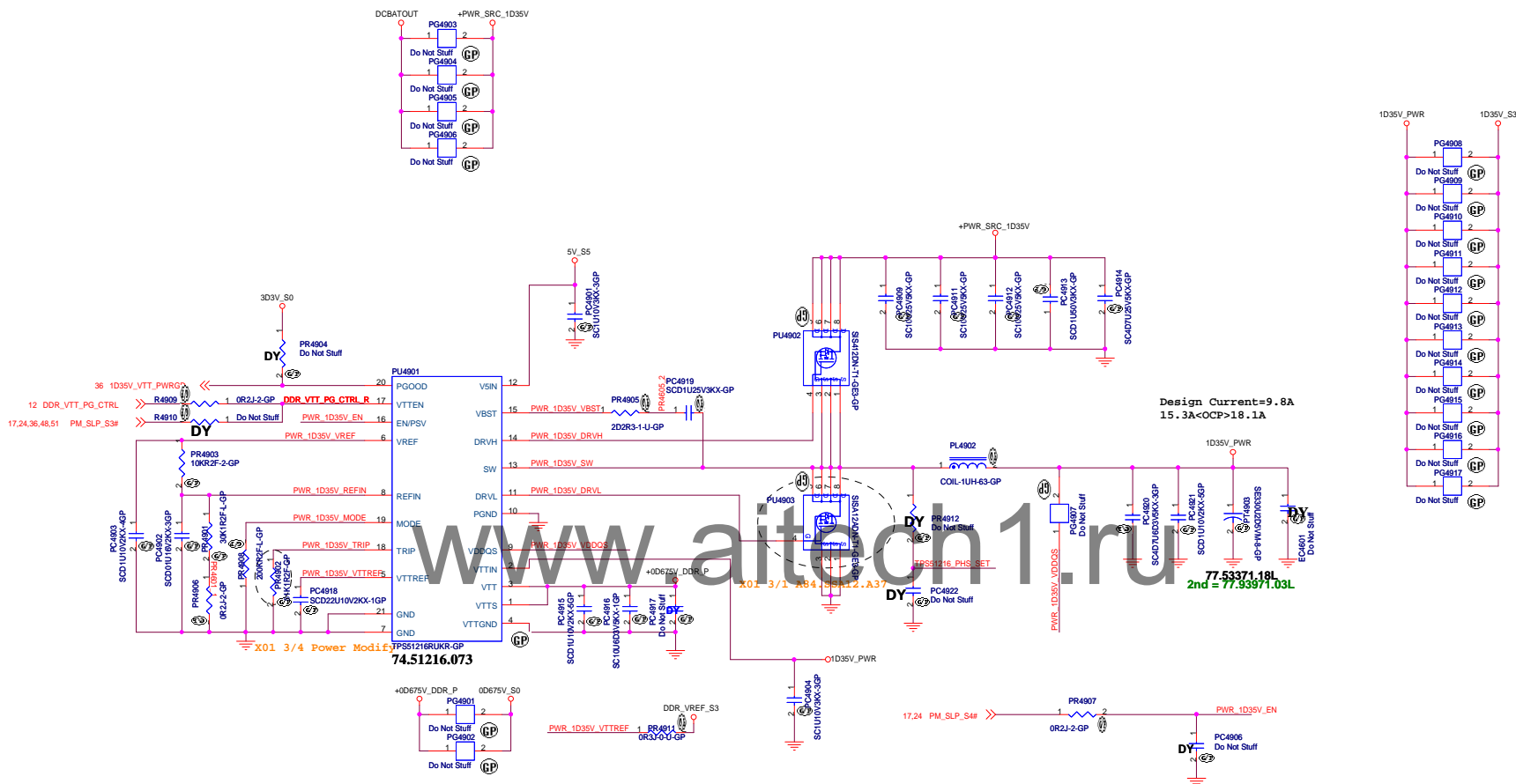


I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18-20mohm Isat =14Arms 68.2R210.20B  
O/P cap: CHIP CAP POL 330U 2.5V M 6.3\*4.5 2.3Arms Matsuti/77.53371.18L  
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S:SIS780DN-T1-GE3 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

$$V_{out} = 0.704V * (R1 + R2) / R2$$

X01 3/1 Powermodifyc

SSID = PWR.Plane.Regulator 1p35v0p675v



| State | S3 | S5 | VDDR | VTTREF | VTT       |
|-------|----|----|------|--------|-----------|
| S0    | Hi | Hi | On   | On     | On        |
| S3    | Lo | Hi | On   | On     | Off(Hi-Z) |
| S4/S5 | Lo | Lo | Off  | Off    | Off       |

## MODE

|          |           |                        |
|----------|-----------|------------------------|
| PR4608   | Frequency | Discharge Mode         |
| 200k ohm | 400kHz    | Tracking Discharge     |
| 100k ohm | 300kHz    |                        |
| 68k ohm  | 300kHz    | Non-tracking Discharge |
| 47k ohm  | 400kHz    |                        |

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP LND 0.1UH M PCMC063T-R10NN 1.5-1.7mohm Isat =60Arms 68.R1010.10T  
O/P cap: CHIP CAP POL 330U 2.5V M 6.3\*4.5 2.3Arms Matsuti/77.53371.18L  
H/S MOS: FET MOS ISi412DN-T1-GE3 NC BP / 84.00412.037 / Rds(on)=24-30mohm @Vgs=4.5V  
L/S MOS: FET MOS ISi780DN-T1-GE3 NC BP POWERPAK 121 / 84.00780.037 / Rds(on)=14.5-17.5mohm @Vgs=4.5V

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Title

**Reserved**

Size  
A3

Document Number  
**Latitude300 Haswell**

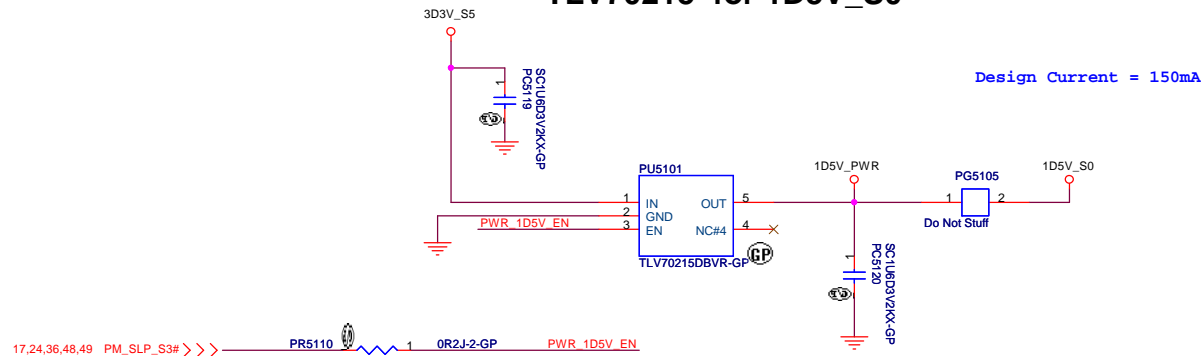
Rev  
**X00**

Date: Friday, March 15, 2013

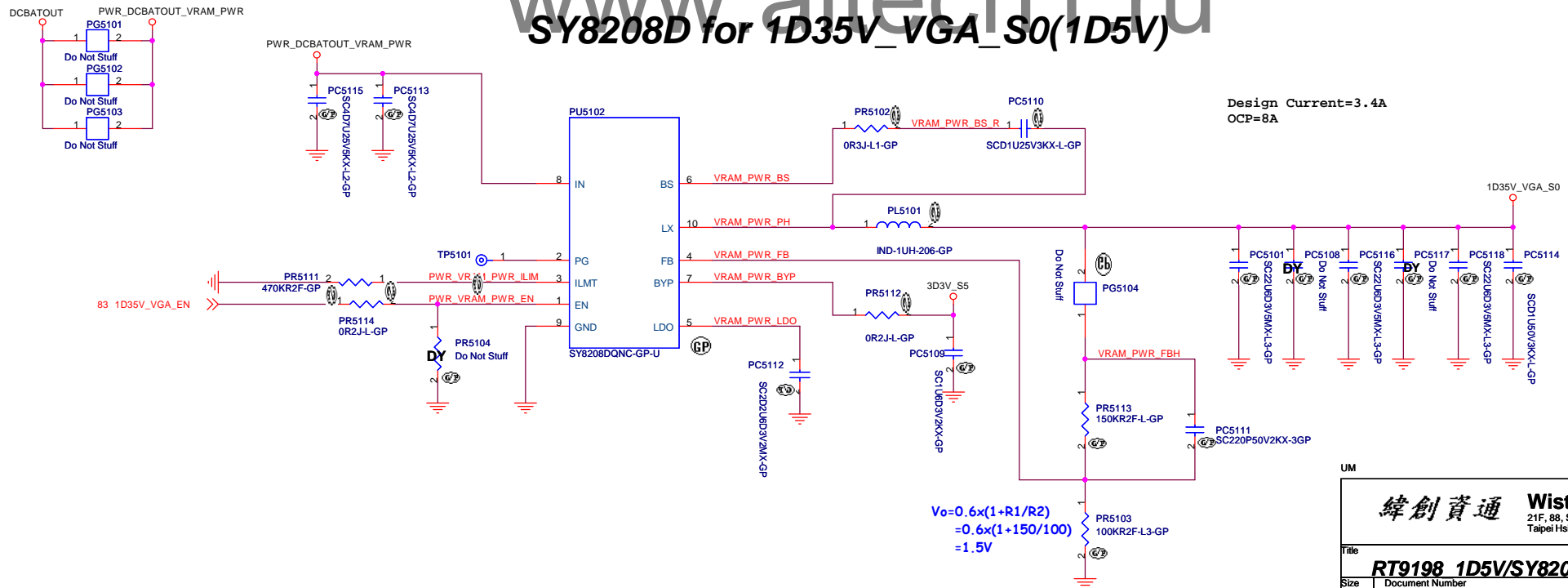
Sheet 50 of 104

```
SSID = PWR.Plane.Regulator_1p5v
```

## TLV70215 for 1D5V\_S0



**SY8208D for 1D35V\_VGA\_S0(1D5V)**



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|                                      |                        |                            |            |
|--------------------------------------|------------------------|----------------------------|------------|
| Title                                |                        |                            |            |
| <b>RT9198 1D5V/SY8208D 1D5V(VGA)</b> |                        |                            |            |
| Size                                 | Document Number        |                            | Rev        |
| A3                                   |                        | <b>Latitude300 Haswell</b> | <b>X00</b> |
| Date:                                | Friday, March 15, 2013 | Sheet 51 of                | 104        |





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Title

**HDMI Level Shifter/Connector**

Size

A3

Document Number

**Latitude300 Haswell**

Rev

**X00**

Date:

Friday, March 15, 2013

Sheet

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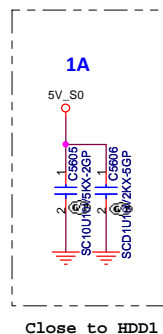
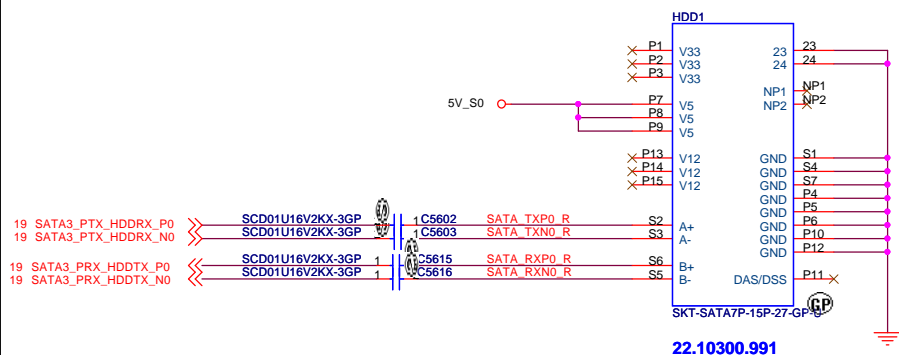
of

104

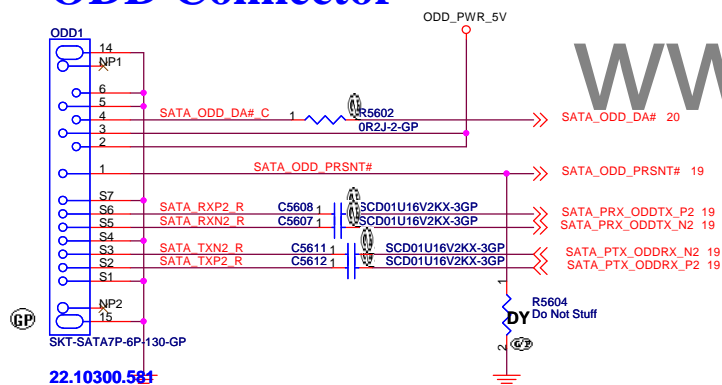


SSID = SATA

## SATA HDD Connector

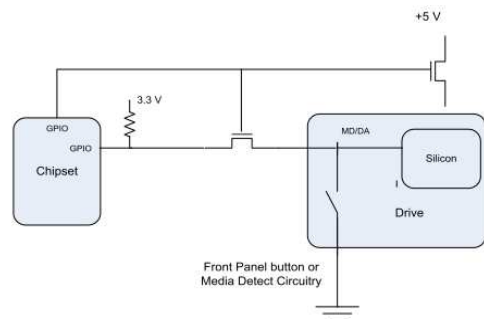
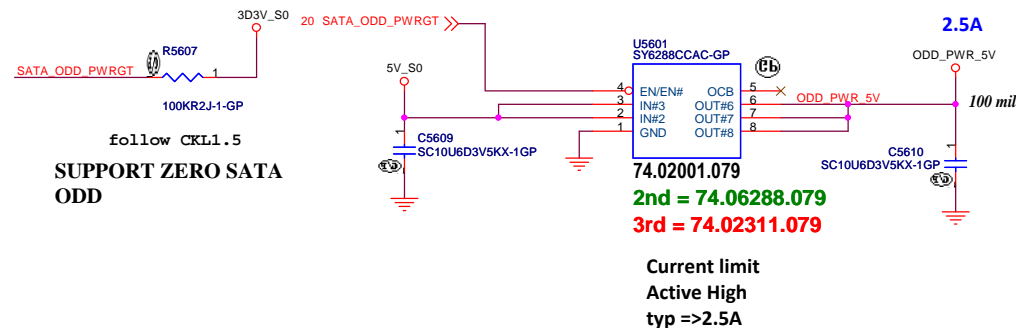


## ODD Connector



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## SATA Zero Power ODD




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SSID = ESATA

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Title

ESATA

Size

A3

Document Number

Latitude300 Haswell

Date: Friday, March 15, 2013

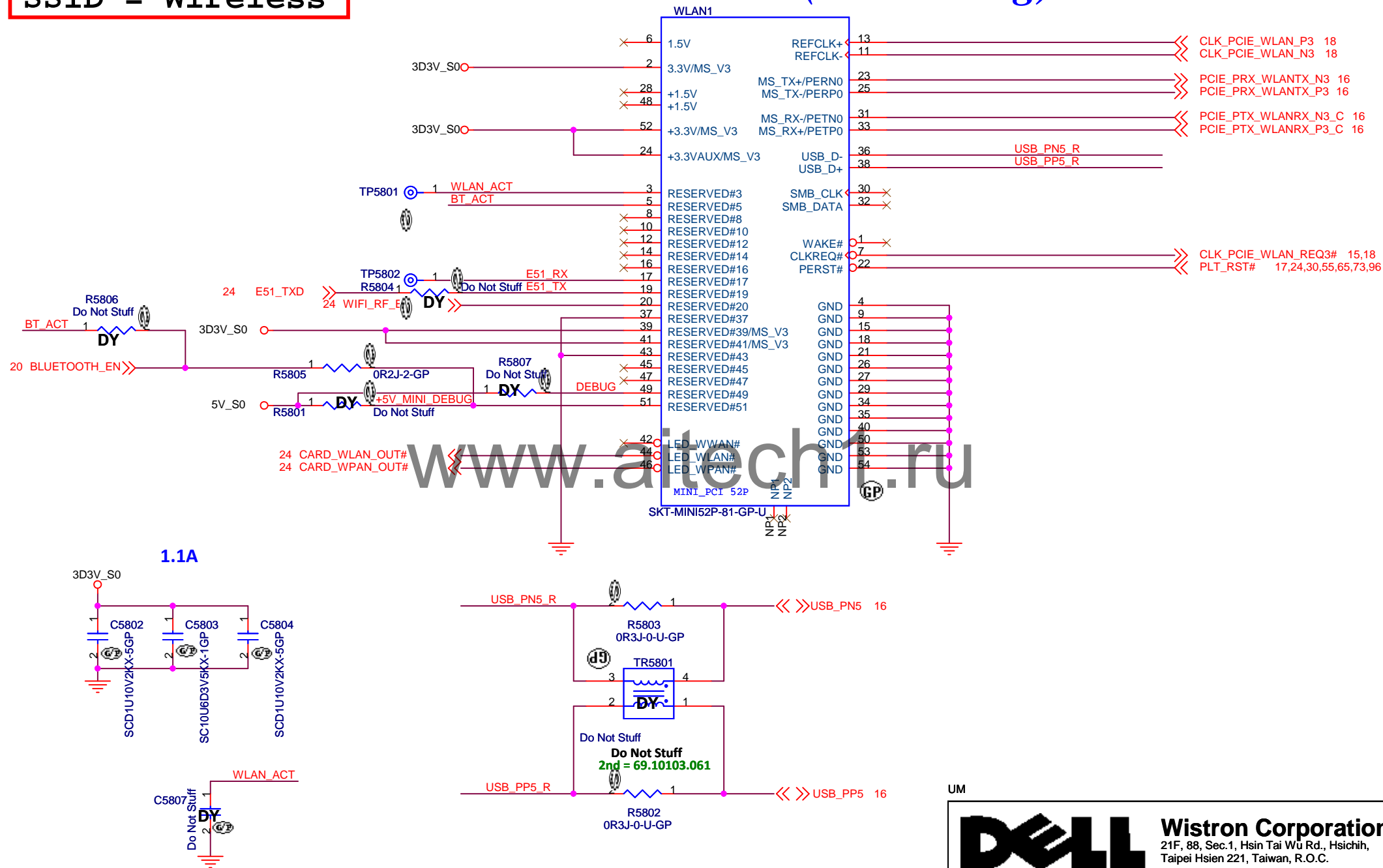
Rev

X00

Sheet 57 of 104

SSID = Wireless

# Mini Card Connector(802.11a/b/g)



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|  |   |                   |
|--|---|-------------------|
| <b>DELL</b> Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |   |                   |
| Title<br><b>MINICARD(WLAN)/ITP CONN</b>  |   |                   |
| Size<br>A4   | Document Number<br><b>Latitude300 Haswell</b> | Rev<br><b>X00</b> |
| Date: Friday, March 15, 2013   | Sheet 58 of 104                               |                   |


(Blanking)

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SSID = PCH

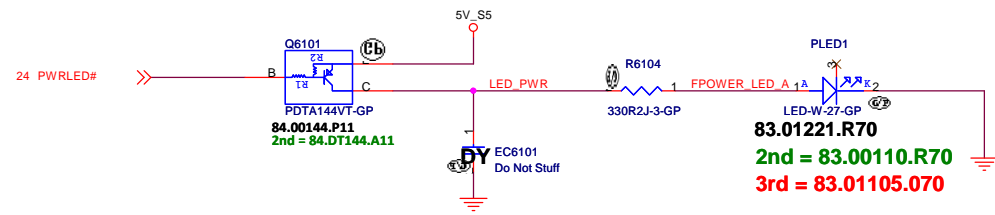
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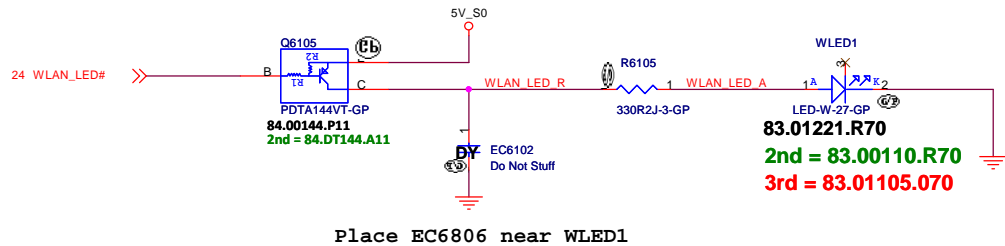
|   |   |   |                   |
|---|---|---|-------------------|
|  |   | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                   |
| Title (Reserved)  |   |   |                   |
| Size<br>A4  | Document Number<br><b>Latitude300 Haswell</b> |   | Rev<br><b>X00</b> |
| Date: Friday, March 15, 2013  |   | Sheet 60 of   | 104               |

SSID = User.Interface

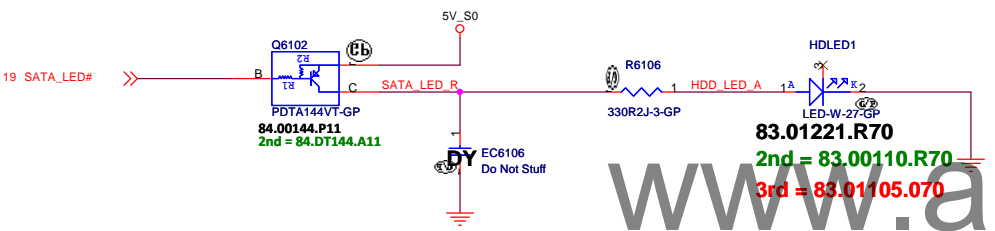
FRONT POWER LED  
Low actived from KBC GPIO



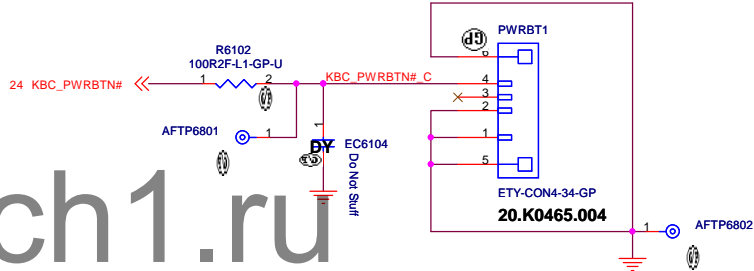
Wireless LED  
Low actived from KBC GPIO



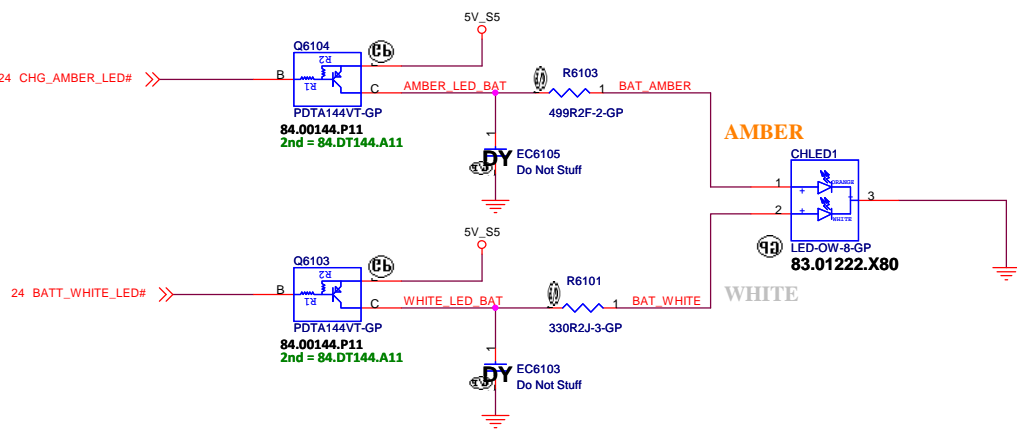
SATA HDD LED(White)  
Low actived from PCH GPIO



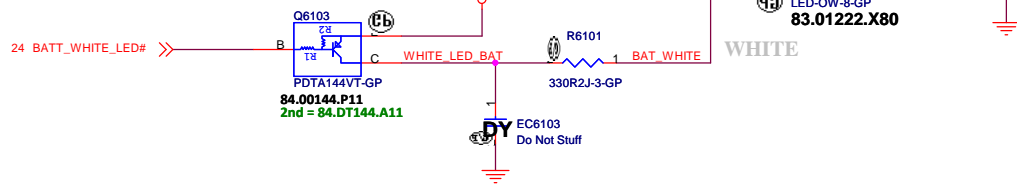
Power button



Battery LED1 (AMBER\_LED)  
Low actived from KBC GPIO



Battery LED2 (WHITE\_LED)  
Low actived from KBC GPIO

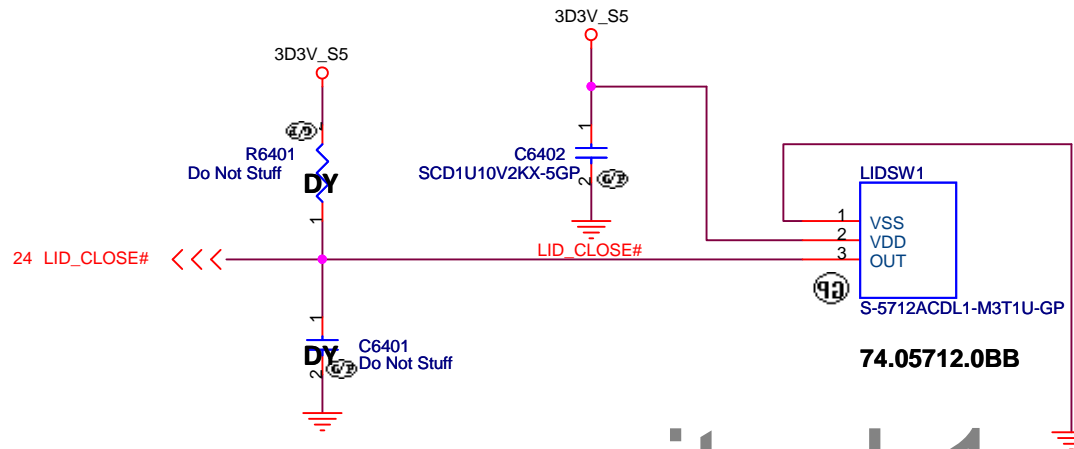




SSID = User.Interface



SSID = User.Interface

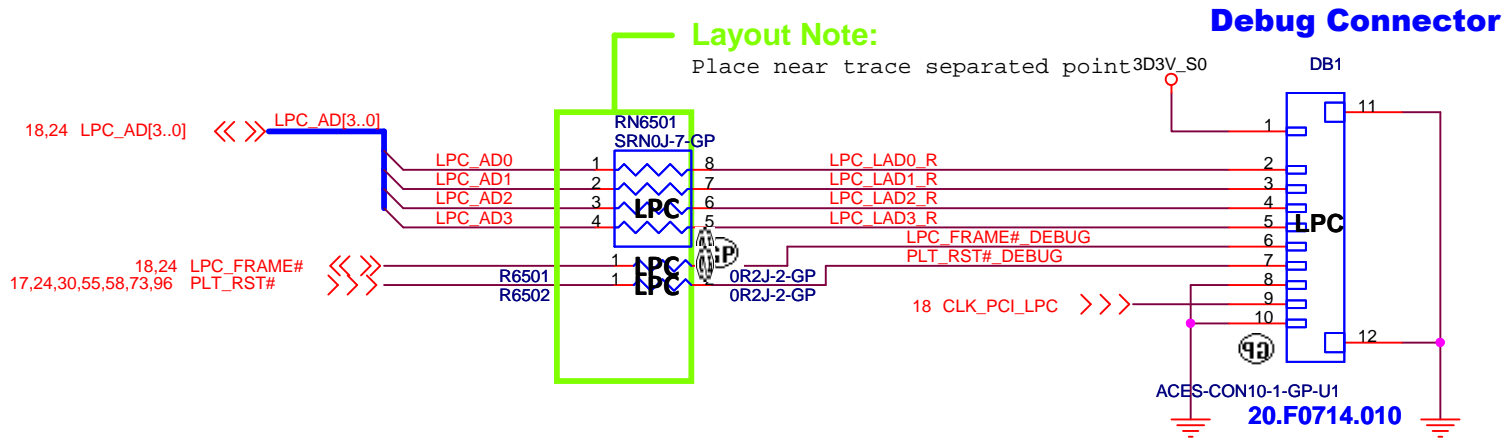


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| Title<br><b>Hall Sensor</b>  |   |   |                   |
| Size<br>A4                   | Document Number<br><b>Latitude300 Haswell</b> |   | Rev<br><b>X00</b> |
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SSID = DEBUG PORT



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Size  
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**X00**


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| A3   | <b>Latitude300 Haswell</b> | <b>X00</b> |

|                              |                 |
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**USB3.0 PORT**


|      |                            |            |
|------|----------------------------|------------|
| Size | Document Number            | Rev        |
| A3   | <b>Latitude300 Haswell</b> | <b>X00</b> |

|                              |                 |
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Size  
A3

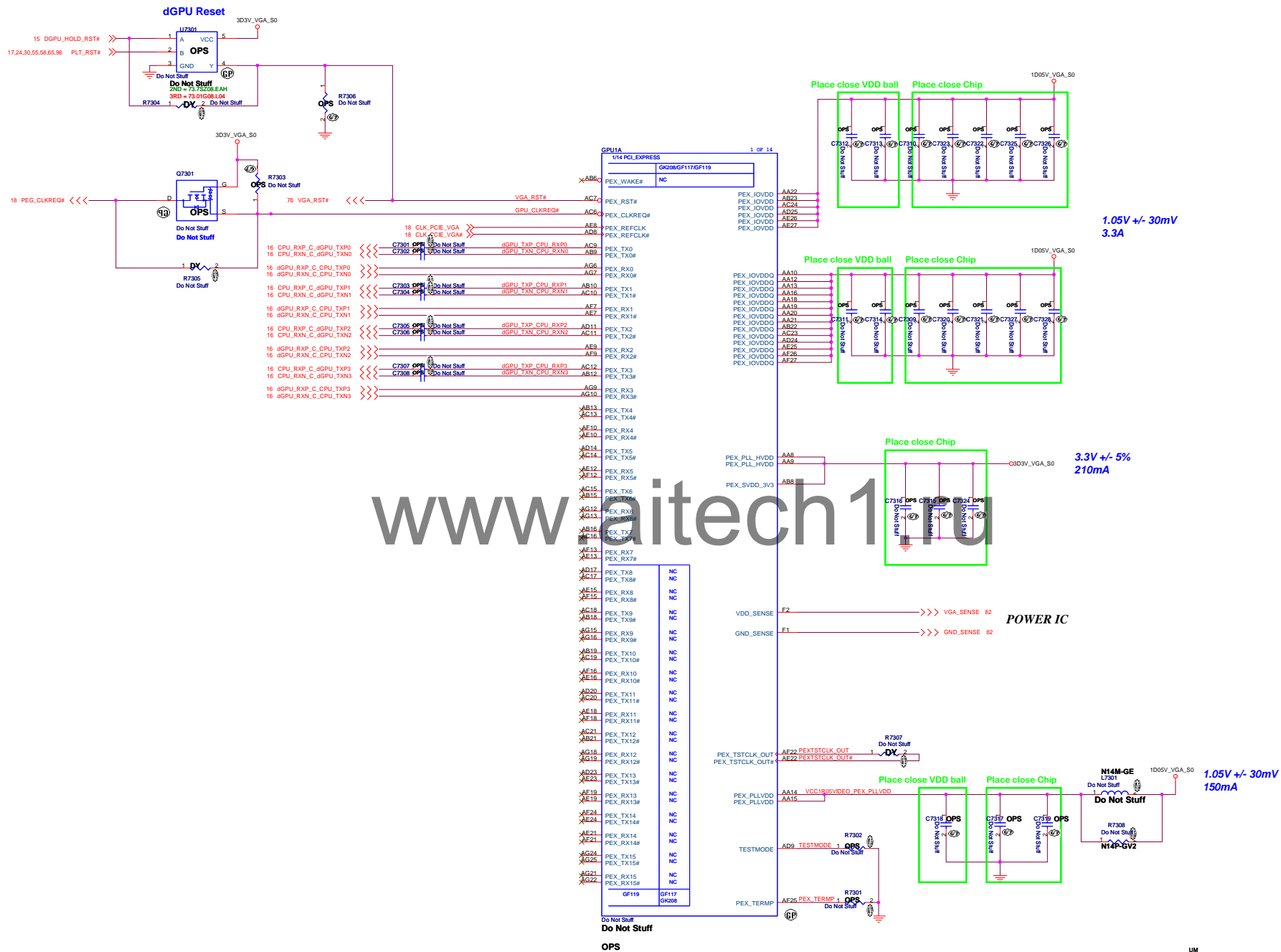
Document Number  
**Latitude300 Haswell**

Rev  
**X00**

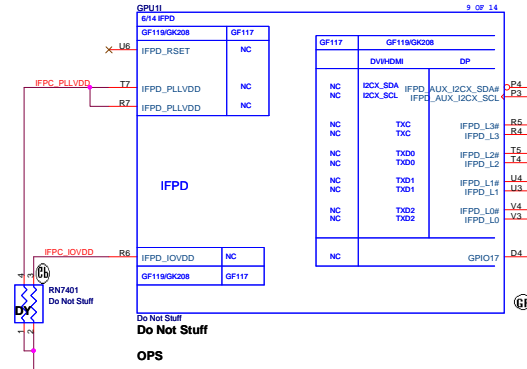
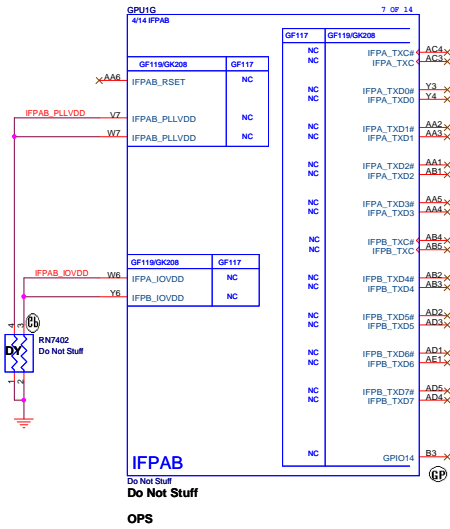
Date: Friday, March 15, 2013

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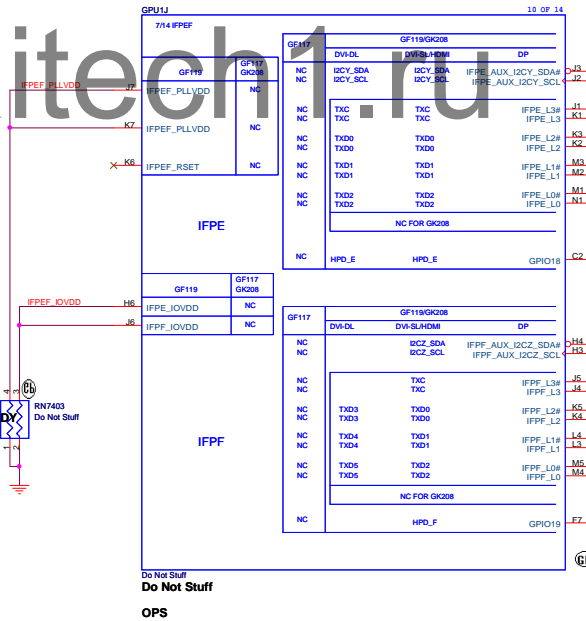
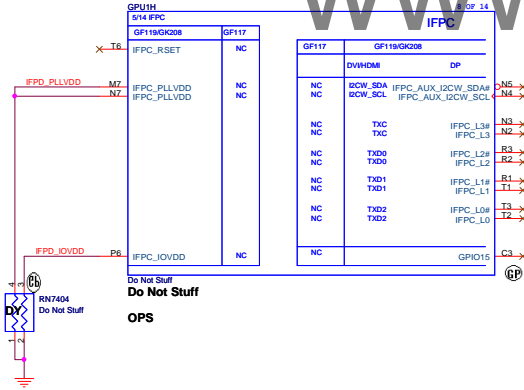
Reserved



## LVDS Interface



## HDMI Interface







| GPU Package Type   | PLL Rail | Capacitor Type   | Footprint | Population | Location  |
|--------------------|----------|--|-----------|------------|-----------|
| G82-64 and G84-128 | PLL_VDD  | 100 nF X7R   | 0402      | 1          | Under GPU |
|                    |          | 22 $\mu$ F X7R   | 0805      | 1          | Neat GPU  |
| <b>Bead Type</b>   |          |  |           |            |           |
|                    |          | 30 $\Omega$ (ESR=0.010 for H+AE-GE; 0.05 for all others) | 0402      | 1          | Neat GPU  |

| GPU Package Type            | PLL Rails      | Capacitor Type | Footprint | Population | Location   |
|-----------------------------|----------------|----------------|-----------|------------|------------|
| GB2-64, GB4-128 and GB3-256 | SP_PLLVDD      | 100 nF         | X7R       | 0402       | Under GPU  |
|                             | and VDD_PLLVDD | 4.7 $\mu$ F    | X5R       | 0402       | 1 Near GPU |
|                             | combined       | 22 $\mu$ F     | X5R       | 0805       | 1 Near GPU |
| <b>Bead Type</b>            |                |                |           |            |            |
| 180 $\Omega$ (ESR=0.2)      |                |                | 0603      | 1          | Near GPU   |

Rx GPU:

|                      |   |
|----------------------|---|
| Multi_Strap_Ref0_GND | N |
| Strap Mode Selected  | B |

N14M-GE

Table 1.

|  |  |
|--|--|
|  |  |
|--|--|

### Configuration

110

|            |
|------------|
| Resistor V |
| 4.99 k     |

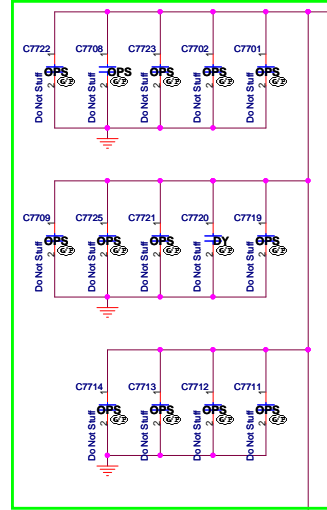
Strap Pin Name

|                |          |
|----------------|----------|
| Strap Pin Name | ROM_SCLK |
|----------------|----------|

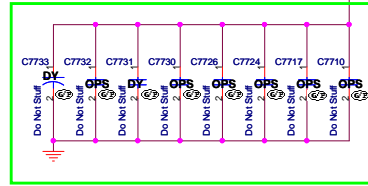
Chip Part

| Strap Pin Name | Long name |
|----------------|-----------|
| ROM_SOLE       |           |

# Under GPU

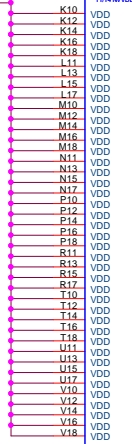


# Near GPU



VGA\_CORE

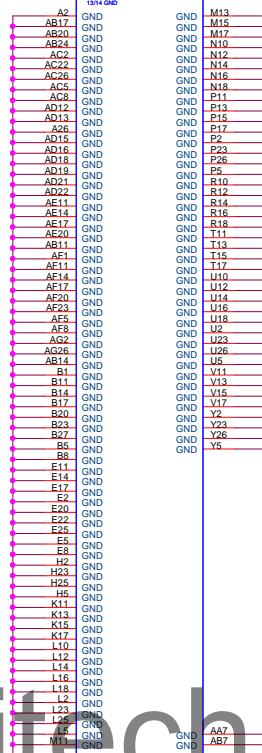
GPU1E 5 OF 14



Do Not Stuff

OPS

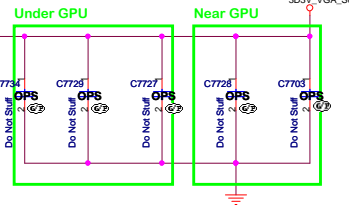
GPU1F 6 OF 14



Do Not Stuff

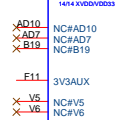
OPS

3.3V +/- 5%  
85mA



303V\_VGA\_S0

GPU1C 3 OF 14



CONFIGURABLE  
POWER CHANNELS  
\* See pin subtable

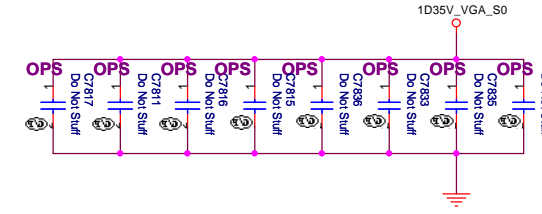
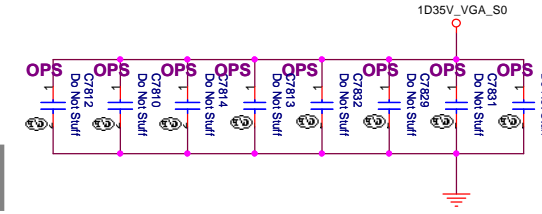
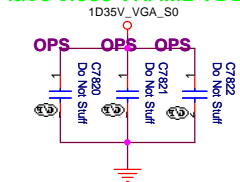
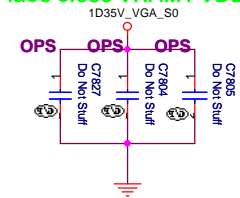
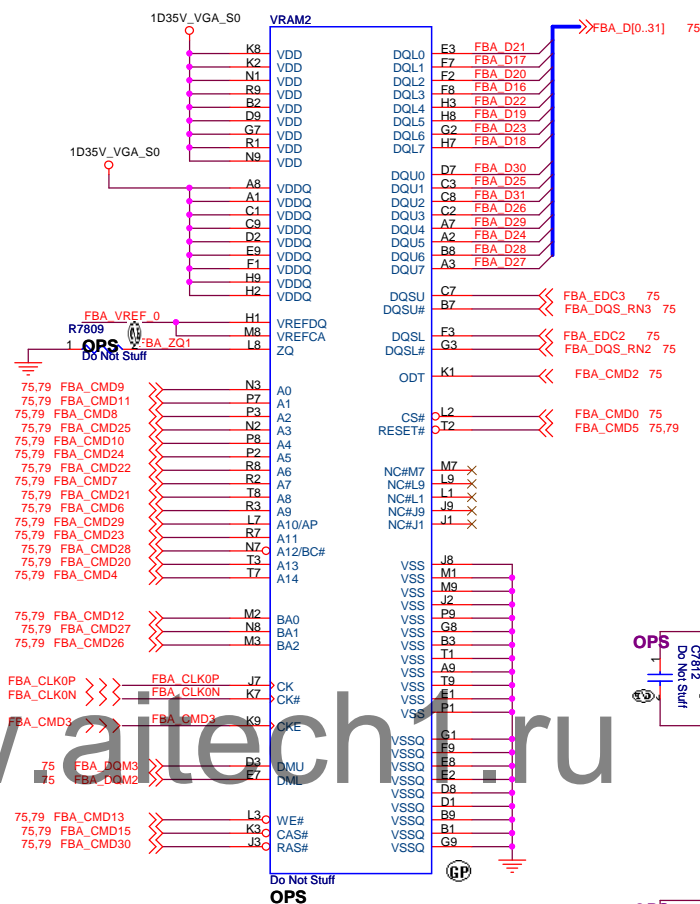


Do Not Stuff

OPS

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| Title <b>GPU DPPWR/GND(5/5)</b>  |  |
| Size Custom  | Document Number <b>Latitude300 Haswell</b> |
| Date: Friday, March 15, 2013   | Sheet 77 of 104                            |



1D35V\_VGA\_S0

R7805  
Do Not Stuff

OPS

R7804  
Do Not Stuff

R7807  
Do Not Stuff

C7805  
OPS

C7806  
OPS

FBA\_VREF\_0

FBA\_VREF\_FET\_L

Q7801  
Do Not Stuff  
**Do Not Stuff**  
**2ND = 84.2N702.031**

DI

DI

GPI010\_FBVREF >>>

Description

| Type           | FBVREF% | Voltage | GPU_GPIO10 |
|----------------|---------|---------|------------|
| Un-termination | 50%     | 0.749V  | High       |
| Termination    | 70%     | 1.0617V | Low        |

| Type           | FBVREF% | Voltage | GPU_GPIO10 |
|----------------|---------|---------|------------|
| Un-termination | 50%     | 0.749V  | High       |
| Termination    | 70%     | 1.0617V | Low        |



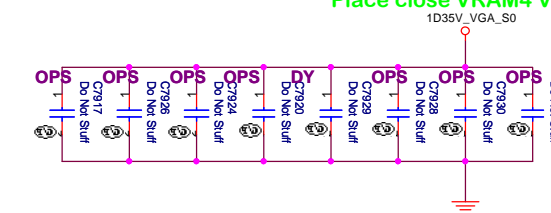
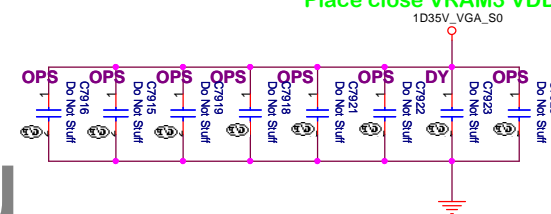
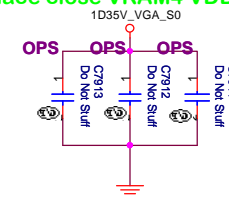
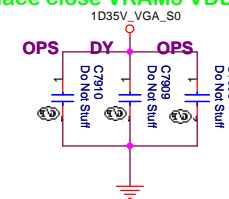
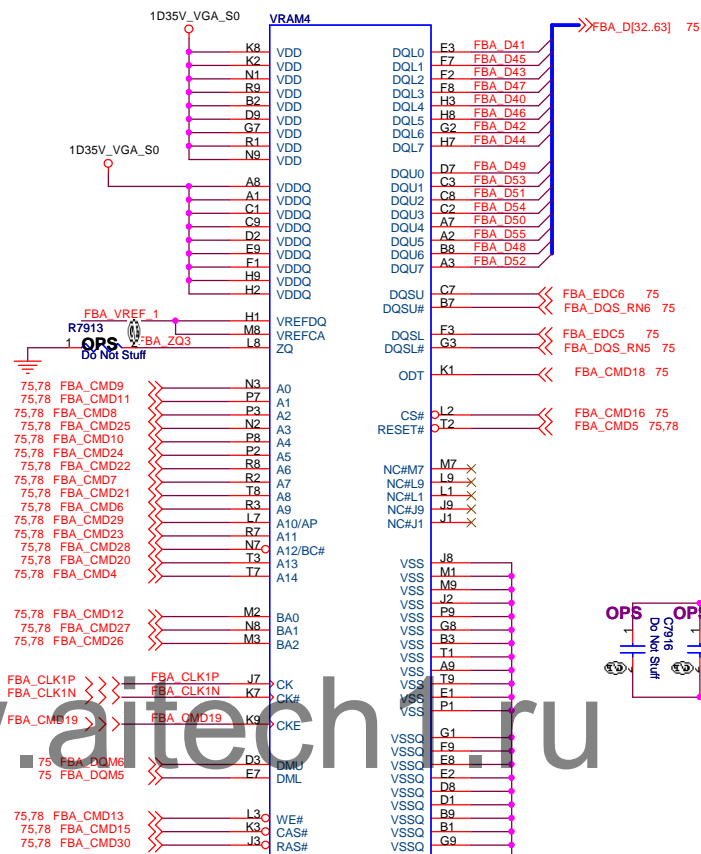
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**GPU-VRAM1,2 (1/4)**

## atitude300 Haswell

|             |     |
|-------------|-----|
| 500 Haswell | X00 |
|-------------|-----|

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1D35V\_VGA\_S0

R7903  
Do Not Stuff

R7902  
Do Not Stuff

R7904  
Do Not Stuff

R7906  
Do Not Stuff  
DY

R7908  
Do Not Stuff  
DY

C7902  
OPS

C7931  
DY

Q7901  
Do Not Stuff  
Do Not Stuff  
2ND = 84.2N702.031

FBA\_VREF\_1

FBA\_VREF\_FET\_H

FBA\_CLK1P

FBA\_CLK1N

GPIO10\_FBVREF

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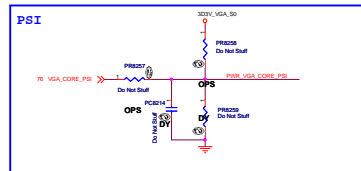
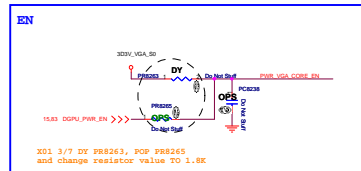
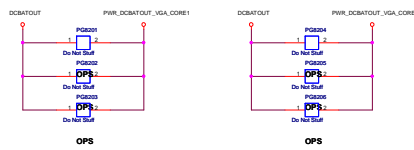
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| <b>GPU-VRAM5,6 (3/4)</b>  |                            |   |                 |
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| A3  | <b>Latitude300 Haswell</b> |   | <b>X00</b>      |
| Date:   | Friday, March 15, 2013     |   | Sheet 80 of 104 |

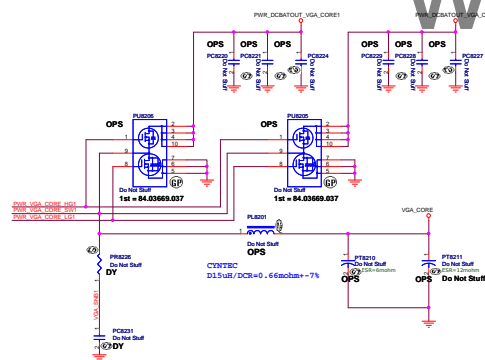
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| <b>GPU-VRAM7,8 (4/4)</b>  |                            |   |                 |
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| A3  | <b>Latitude300 Haswell</b> |   | <b>X00</b>      |
| Date:   | Friday, March 15, 2013     |   | Sheet 81 of 104 |

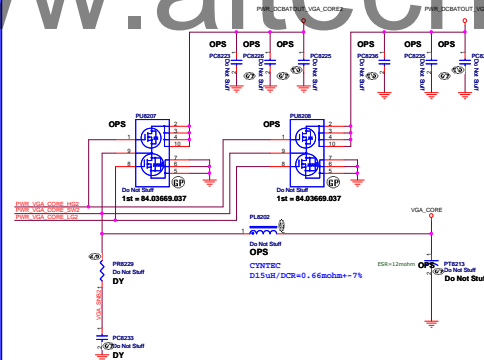


#### Phase1



I/P cap: 100 25V K8005 XSR/ 78.10622.511.  
 MOS: Q1: Id=10A, Rds(on)=9.8-13.2 mohm / Q2: Id=17A, Rds(on)=3.6-5.2mohm 84.03669.037  
 Inductor: CHIP CHOKE 0.22mH PCB0693T-R22M0 2.5-3mohm Isat =34Arms 68.R2210.20C  
 O/P cap: CHIP CAP POL 3300 2.5V M 6.3\*4.5 2.3Arms Matsuti/77.53371.18L

#### Phase2



I/P cap: 100 25V K8005 XSR/ 78.10622.511.  
 MOS: Q1: Id=10A, Rds(on)=9.8-13.2 mohm / Q2: Id=17A, Rds(on)=3.6-5.2mohm 84.03669.037  
 Inductor: CHIP CHOKE 0.22mH PCB0693T-R22M0 2.5-3mohm Isat =34Arms 68.R2210.20C  
 O/P cap: CHIP CAP POL 3300 2.5V M 6.3\*4.5 2.3Arms Matsuti/77.53371.18L

EDC=45A  
 EDP=72A

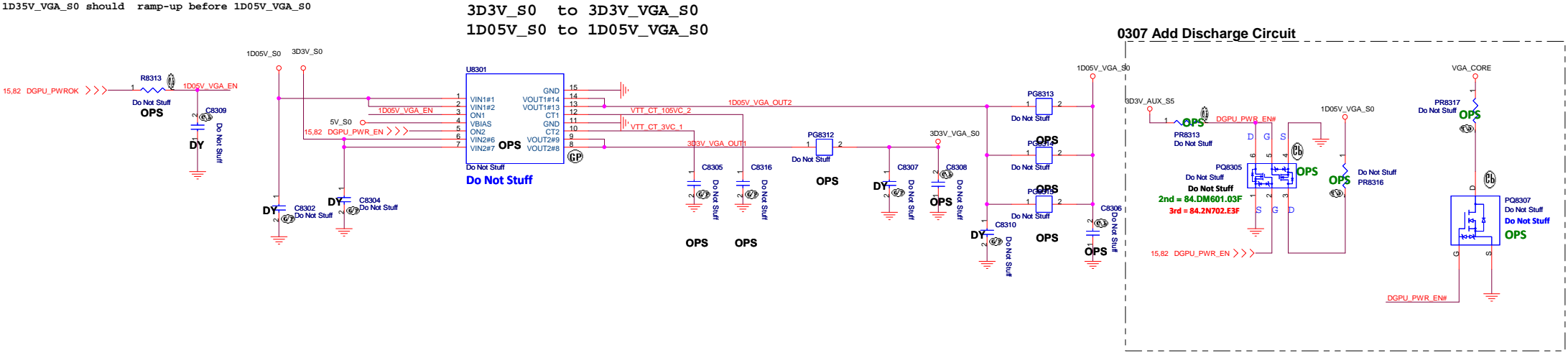
| TYPE     | config | TDC | SDP | OCF | R1/PR8207 | R2/PR8211 | R3/PR8204 | R4/PR8209 | R5/PR8201 | C/PC8219 |
|----------|--------|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|----------|
| N14M-GE  | C      | 35A | 41A |     | 39kohm    | 30kohm    | 3kohm     | 24kohm    | 3kohm     | 1.8nF    |
| N14P-GV2 | B      | 32A | 55A |     | 20kohm    | 20kohm    | 2kohm     | 18kohm    | 0ohm      | 2.7nF    |
| N14P-GT  | B      | 45A | 75A |     | 20kohm    | 20kohm    | 2kohm     | 18kohm    | 0ohm      | 2.7nF    |

Table 1. PWM-VID Spec and Component Values

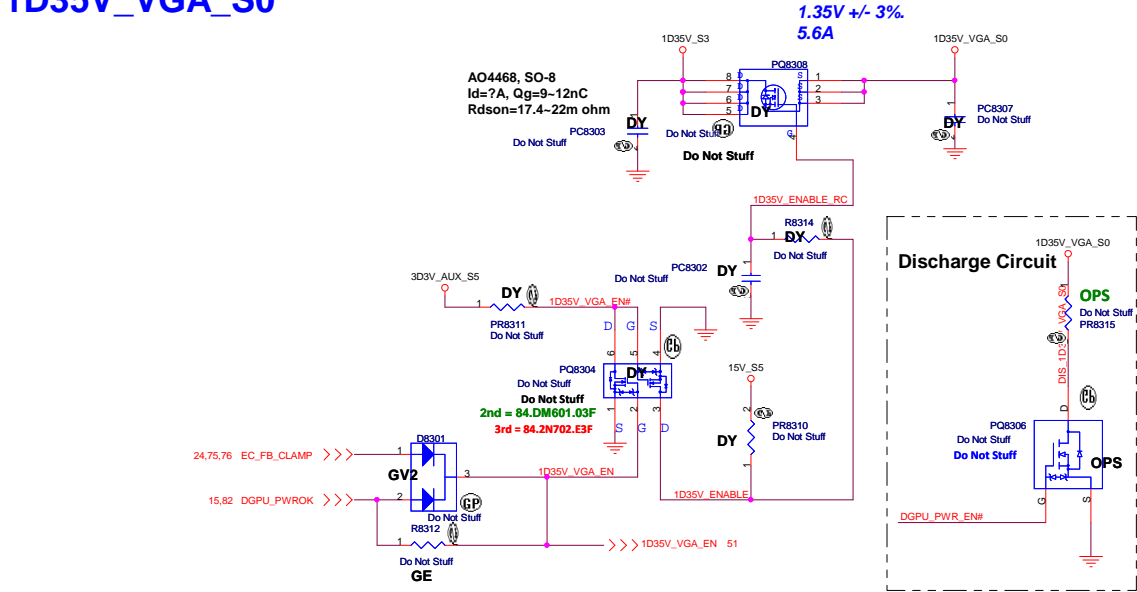
| PWM-VID Spec                               |       | Config A | Config B | Config C |
|--|-------|----------|----------|----------|
| Vmin                                       | V     | 0.6      | 0.6      | 0.65     |
| Vmax                                       | V     | 1.2      | 1.2      | 1.15     |
| Vboot                                      | V     | 0.875    | 0.9      | 0.9      |
| Voltage Step Vstep                         | mV    | 6.25     | 6.25     | 3.5      |
| Number of Voltage Levels N                 | level | 96       | 96       | 20       |
| PWM Frequency F <sub>SW</sub>              | MHz   | 1.125    | 1.125    | 0.676    |
| PWM Minimum Pulse Width T <sub>ONMIN</sub> | ns    | 9.26     | 9.26     | 74       |
| VID Transient Time T                       | us    | <100     | <100     | <100     |
| Component Value                            |       |          |          |          |
| R1 (1%)                                    | kΩ    | 39       | 20       | 39       |
| R2 (1%)                                    | kΩ    | 39       | 20       | 30       |
| R3 (1%)                                    | kΩ    | 1.5      | 2        | 3        |
| R4 (1%)                                    | kΩ    | 30       | 18       | 24       |
| R5 (1%)                                    | kΩ    | 1.5      | 0        | 3        |
| C  | nF    | 1.5      | 2.7      | 1.8      |

3D3V\_VGA\_S0  
1D05V\_VGA\_S0

3D3V\_VGA\_S0 should ramp-up before VGA\_Core  
VGA\_Core should ramp-up before 1D05V\_VGA\_S0  
1D35V\_VGA\_S0 should ramp-up before 1D05V\_VGA\_S0



1D35V\_VGA\_S0




| CtX (pF) | Rise Time (µs) 10% - 90%, COUT = 0.1µF @ VIN; VOUT=0 ohm load |       |      |      |      |       |      |      |
|----------|---|-------|------|------|------|-------|------|------|
|          | Typical values @ 25°C, 25V X7R 10% ceramic cap                |       |      |      |      |       |      |      |
|          | 5V  | 3.3V  | 1.8V | 1.5V | 1.2V | 1.05V | 1V   | 0.8V |
| 0        | 107   | 72    | 46   | 41   | 36   | 34    | 33   | 29   |
| 220      | 425   | 276   | 146  | 122  | 103  | 91    | 88   | 74   |
| 270      | 489   | 316   | 172  | 139  | 121  | 107   | 104  | 84   |
| 470      | 774   | 487   | 272  | 224  | 181  | 159   | 154  | 123  |
| 680      | 1108  | 708   | 375  | 317  | 242  | 221   | 213  | 168  |
| 1000     | 1561  | 1007  | 546  | 441  | 364  | 314   | 299  | 234  |
| 2200     | 3600  | 2289  | 1240 | 1019 | 817  | 681   | 665  | 539  |
| 4700     | 7757  | 5092  | 2674 | 2203 | 1808 | 1592  | 1516 | 1177 |
| 10000    | 15700   | 10310 | 5601 | 4659 | 3674 | 3401  | 3197 | 2562 |

Table 1. Rise time vs. CtX value

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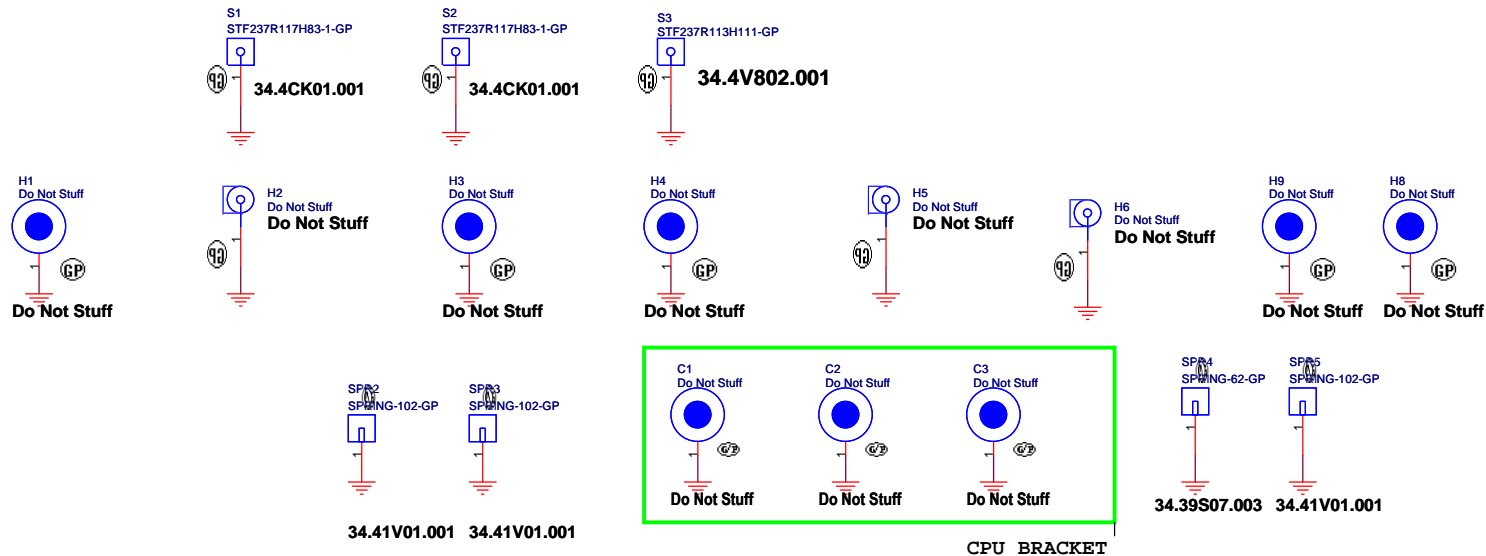
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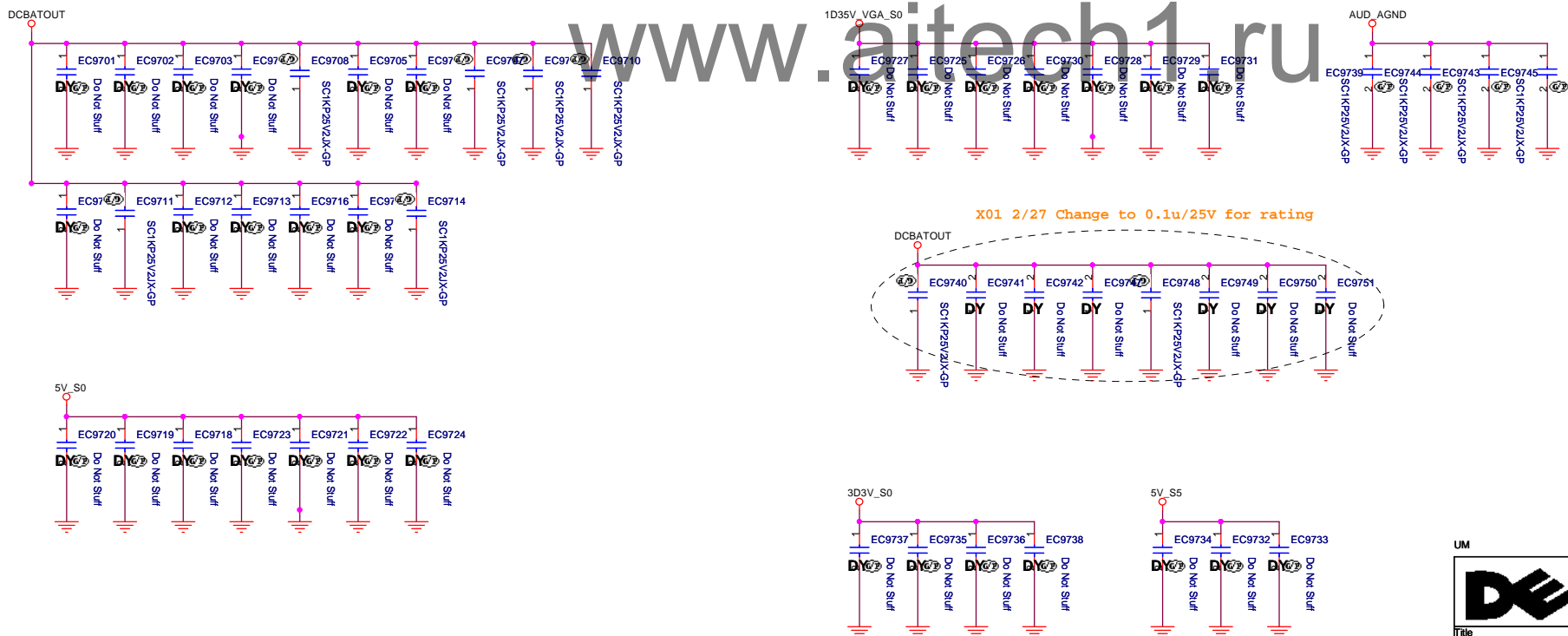
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## SSID = Mechanical



## SSID = EMI



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***LVDS Switch***

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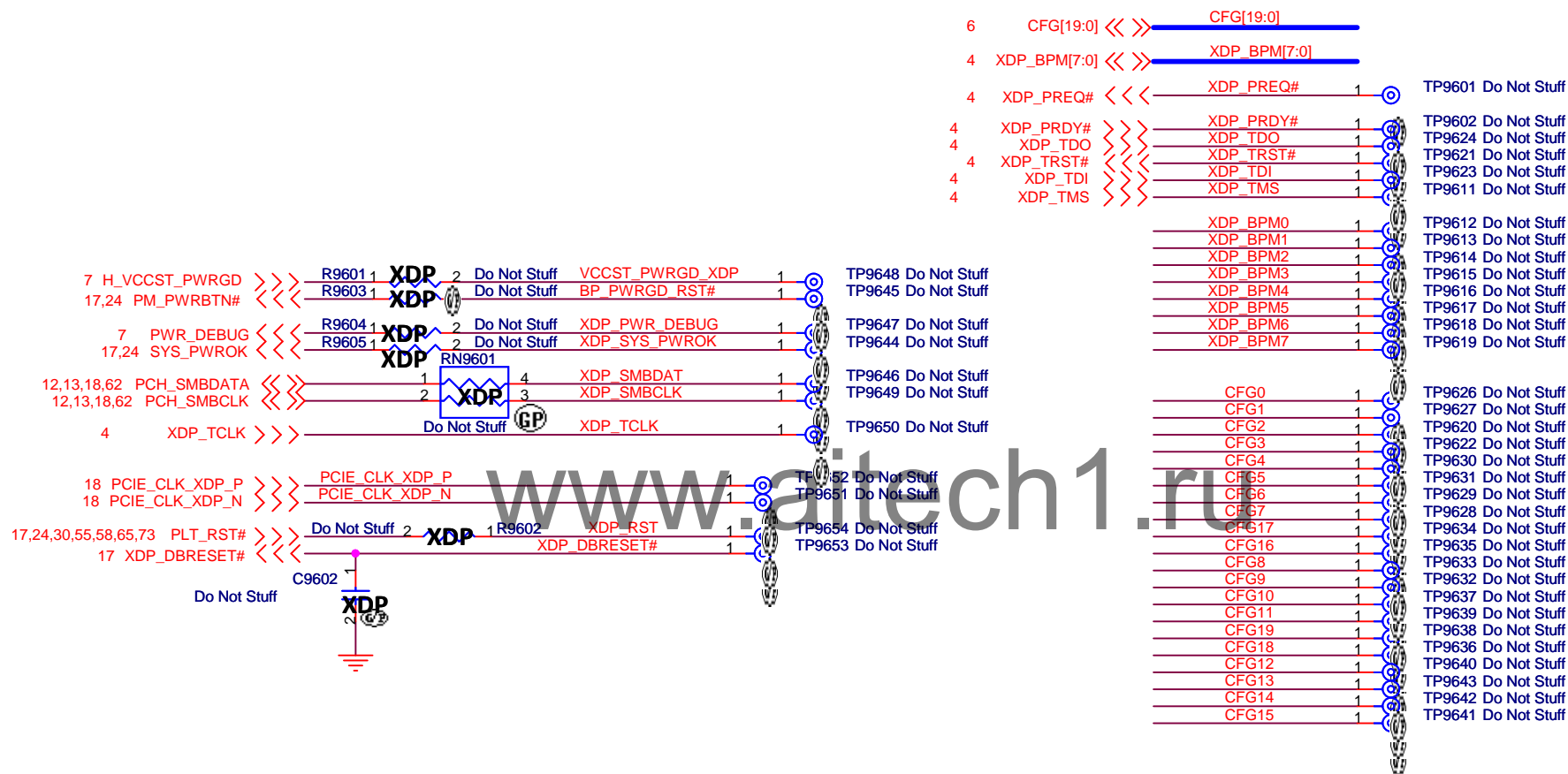
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| <b>CRT Switch</b>   |                            |  |   |    |            |
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**SSID = XDP**

## CPU XDP



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## TOUCH PANEL

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## Latitude300 Haswell

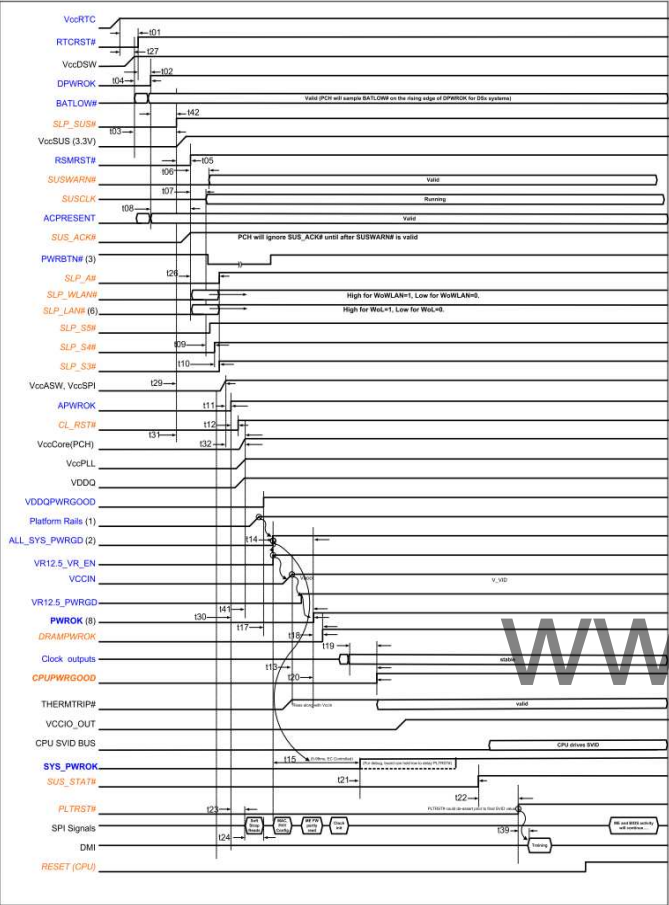
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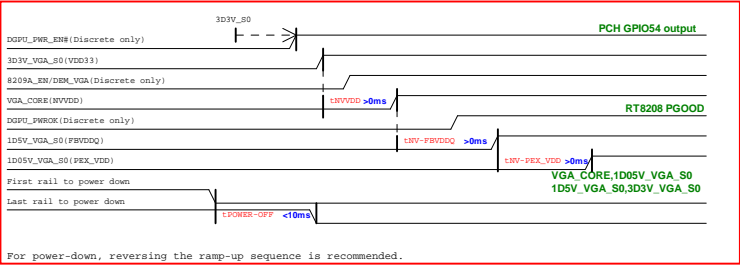
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Shark Bay Platform Power Sequence



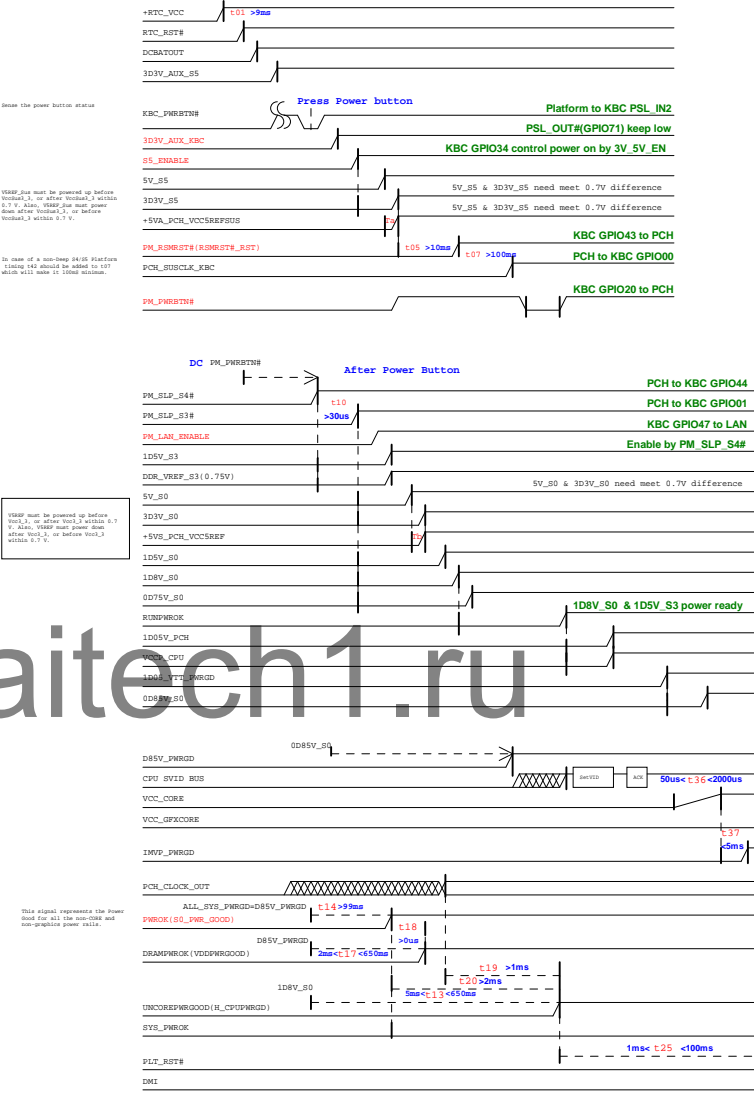
N14P-GT Power-Up/Down Sequence



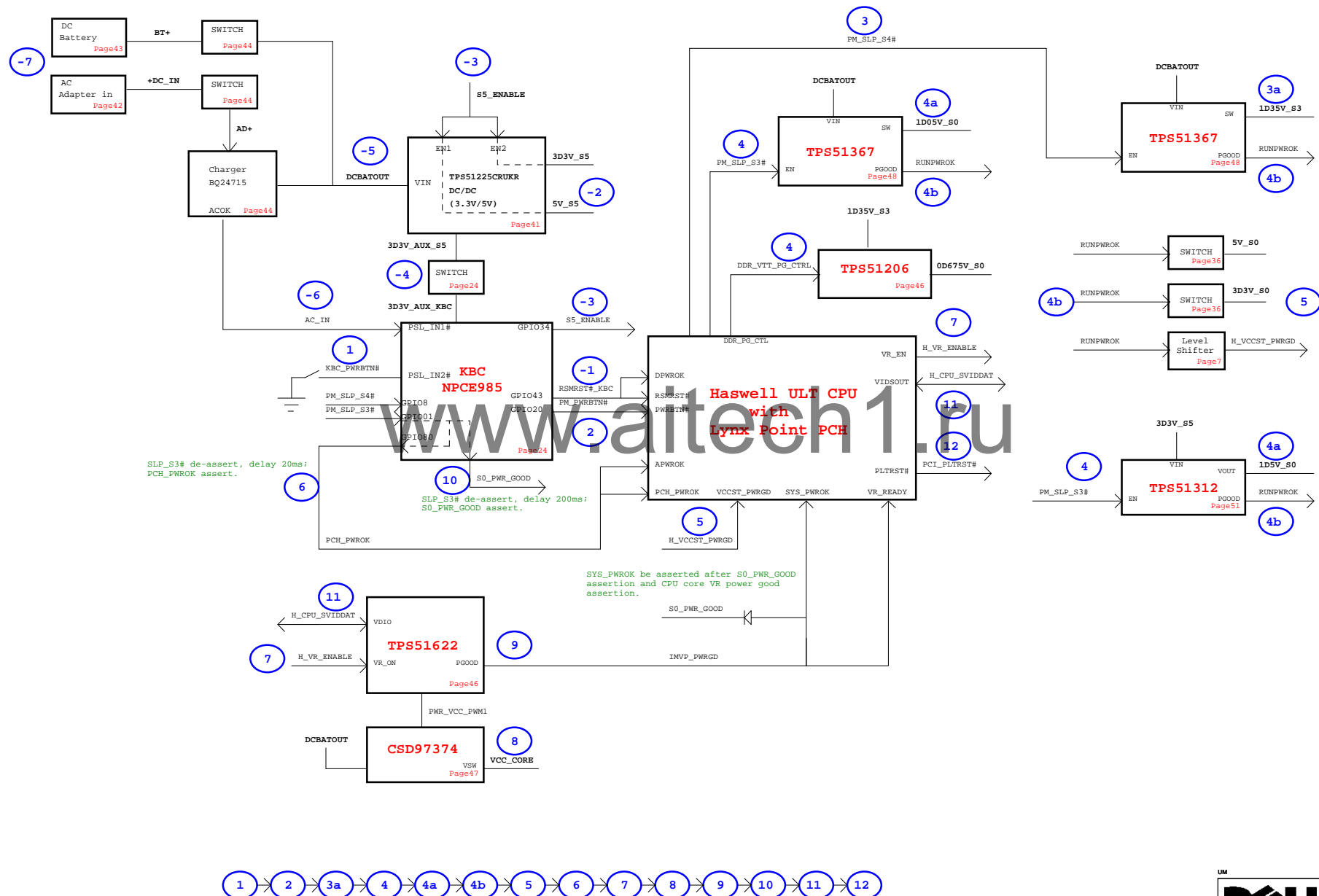
For power-down, reversing the ramp-up sequence is recommended.

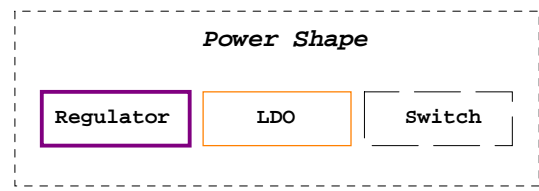
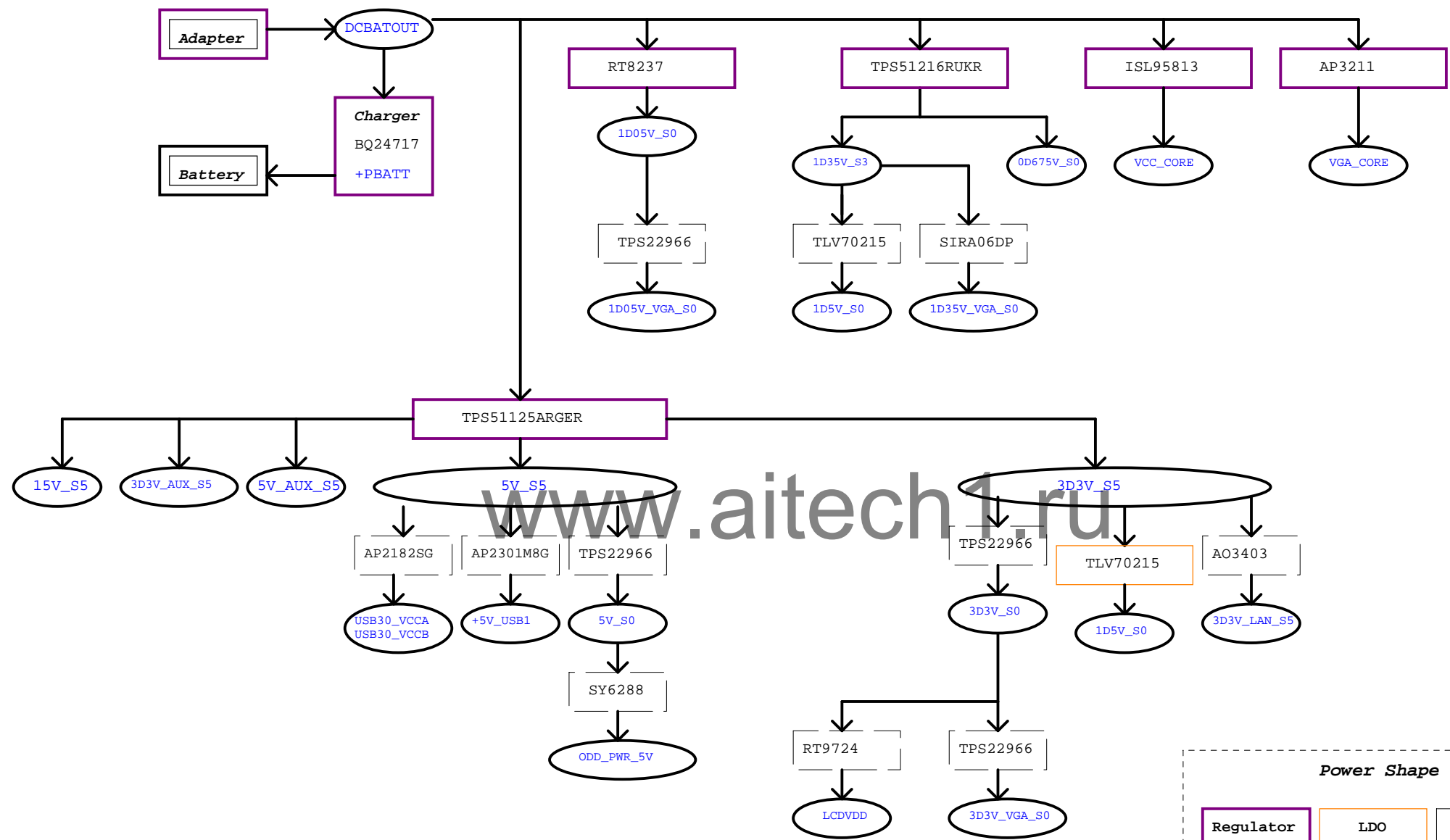
(DC mode)

Red Words: Controlled by EC GPIO

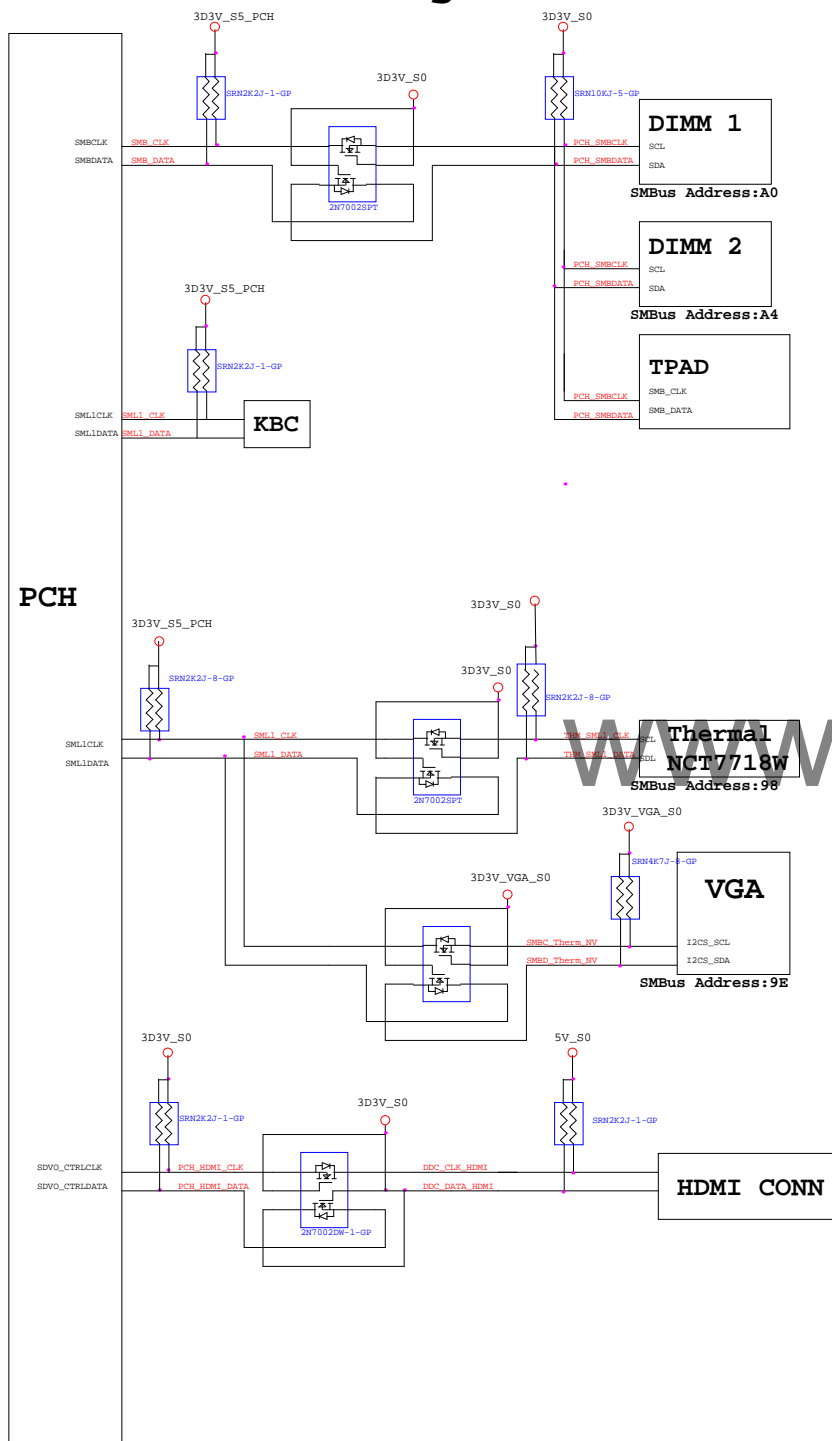


## WISTRON SHARK BAY POWER UP SEQUENCE DIAGRAM

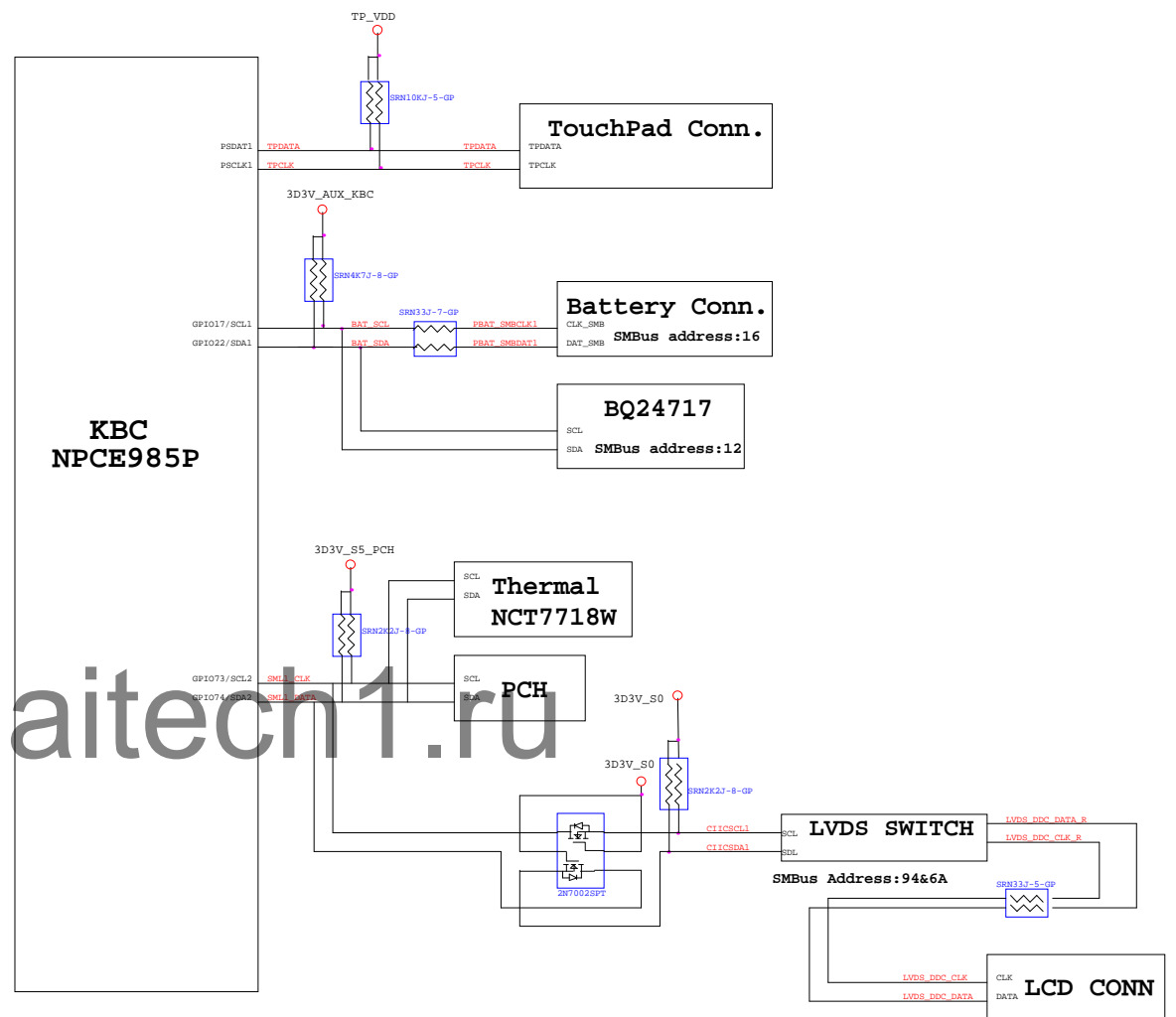




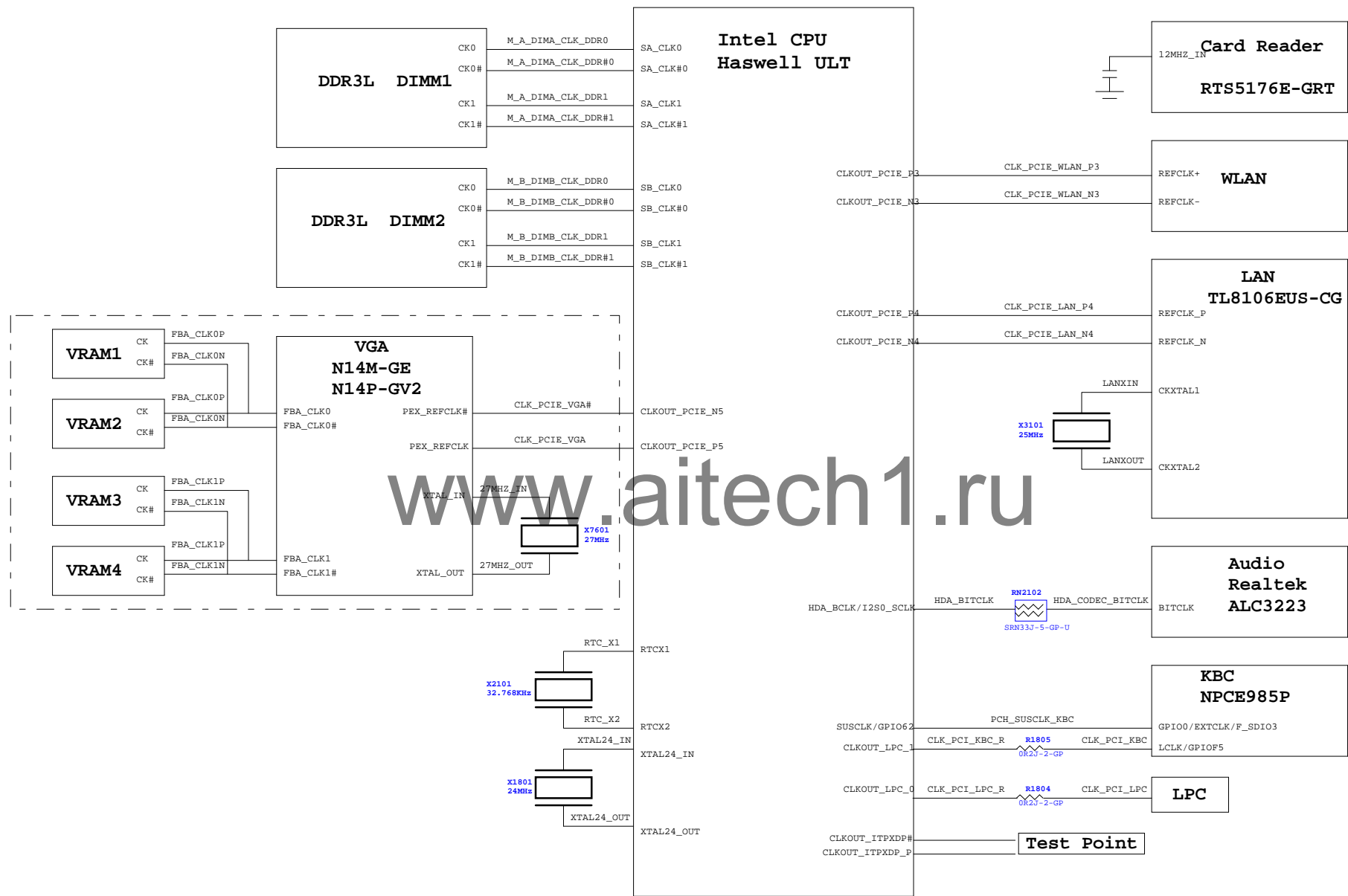
# PCH SMBus Block Diagram



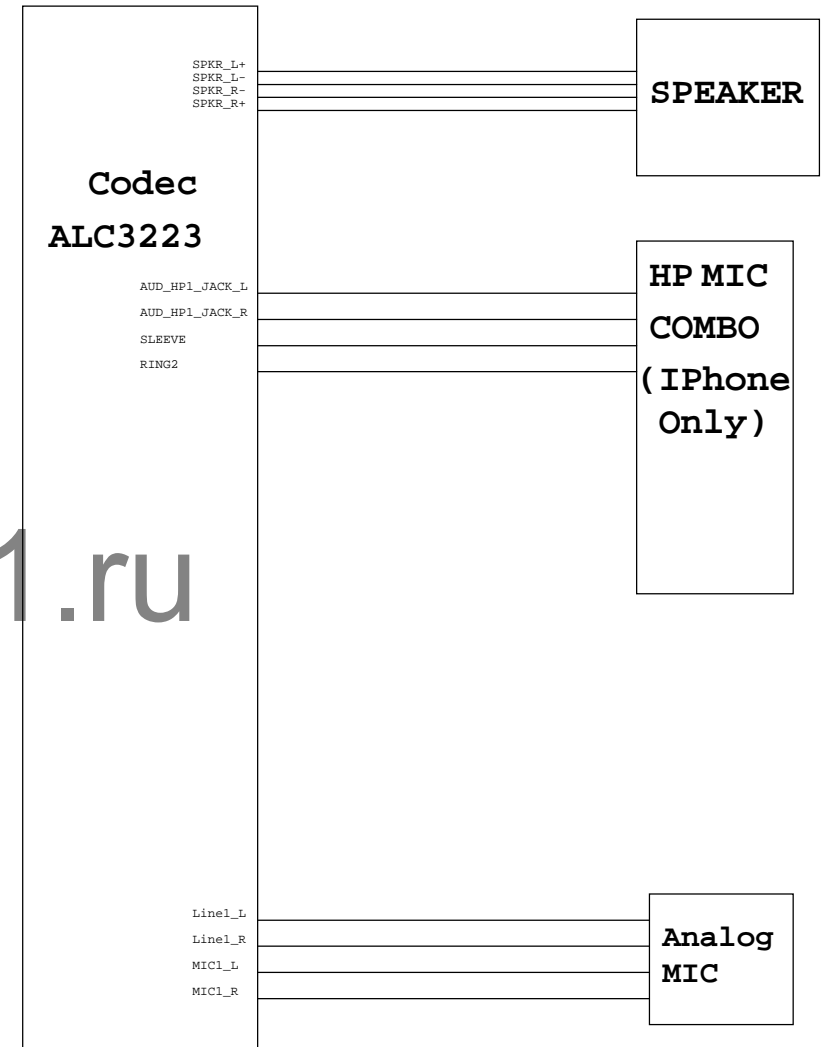
# KBC SMBus Block Diagram



OAK Haswell CLK Block Diagram



## Audio Block Diagram






|         |      |      |             |   |   |   |   |
|---------|------|------|-------------|---|---|---|---|
| 5       |      |      |             | 4 | 3 | 2 | 1 |
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